SONY®

VIDEOCASSETTE RECORDER

BVU-950

Professional U-matic SP

THEORY OF OPERATION

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SECTION 1
OUTLINE

1-1. OUTLINE

This machine is a multi-functional U-matic editor with high picture and sound quality. High picture quality is realized through the use of SP format and high sound quality through a Dolby NR system. A plug-in TBC and time code reader/generator, etc. are available as options for increasing its function and performance. This lowers the cost of the VTR and the same time allows the user to choose only the necessary options. This permits a total editing system to be supplied at a low cost.

The performance of this machine when equipped with the optional accessaries is equivalent to the BVU-850 and its functions exceed the BVU-850. Also its size is the 5 span size, the same as the type 5 series, and with the plug-in TBC installed, it can be exchanged for the current type 5.

	ITEM			BVU-950	COMPARISON	
					BVU-850	BVU-800
EDITING	JOG			O	O	O
	VTR-VTR CONTROL			O	O	O
	CONTROL PANEL EXTENSION			O	O	O
	REMOTE CONTROL CONNECTOR		9P	O	O	O
			24P	O	×	×
			33P	×	×	×
			36P	×	O	O
	TC	READER & GENERATOR		O (BKU-906)	O (BK-806)	O (BK-806)
		FRONT PANEL CONTROL		O (BKU-906)	×	×
		TIME CODE RESET		O (BKU-906)	×	×
		CONNECTOR		BNC	BNC	RCA-PIN
VIDEO	SP	REC		O	O	×
		PB		O	O	O
	CONV	REC		O	O	O
		PB		O	O	O
	TBC	18P MULTI		×	O	O
		BUILT IN		O	×	×
		REMOTE CONNECTOR		O	×	×

Table 1-1

The following models are available as optional accessories.

- BKU-901/901A : NTSC plug-in TBC
- BKU-902 : Digital noise reducer (DNR)
- BKU-905 : NTSC plug-in time code generator/reader
- BKU-906 : Cabinet extension kit
- RMM-950/RMM-501 : Rack mounting kit
- BK-803 : Control panel case
- RCC-10G/30G : 9-pin remote cable

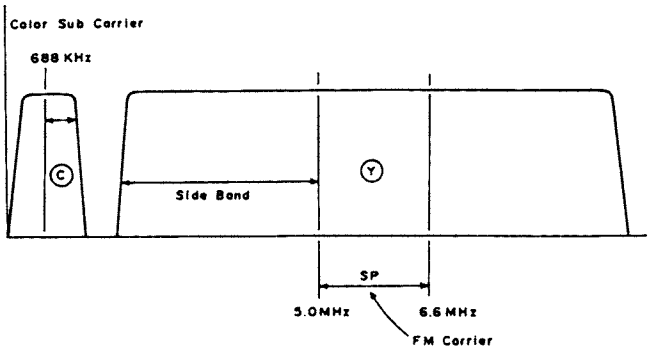
	ITEM			BVU-950	COMPARISON	
					BVU-850	BVU-800
AUDIO	BALANCED XLR AUDIO			O	O	O
	DOLBY (SP MODE)		REC	O (MANUAL)	O (MANUAL)	×
			PB	O (AUTO)	O (AUTO)	×
	AUDIO MIXING			×	O	O
	LEVEL CONTROL		REC	O	O	O
			PB	O	O	O
ETC	DIAL SETTING	CHARACTOR DISPLAY		O	×	×
		TITLE REC		O	×	×
		SELF DIAGNOSTICS		O	×	×
	UNIT SIZE			5	6	6

Table 1-2

1-2. SP FORMAT

In the SP format, the FM carrier frequency of the Y signal is higher than the previous model.

SP FORMAT



CONVENTIONAL FORMAT

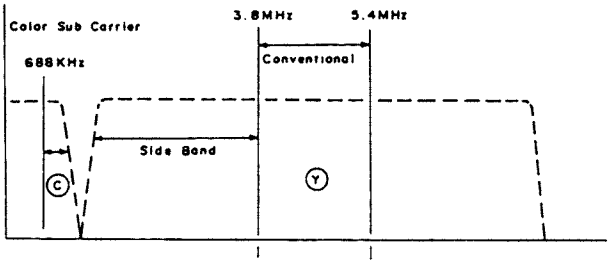


Fig.1-1. SP Format

1-3. SP TAPE

The SP mode is activated only when the SP tape is loaded into SP U-matic VTRs. There are the following six types of SP tape.

- KSP-10
- KSP-20
- KSP-30
- KSP-60
- KSP-S10
- KSP-S20

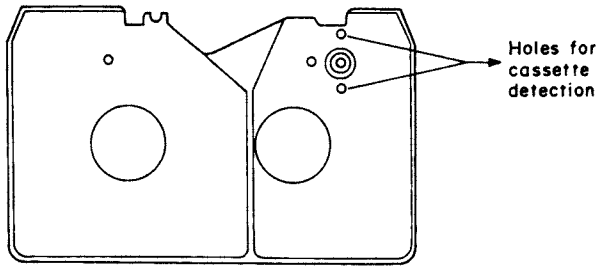
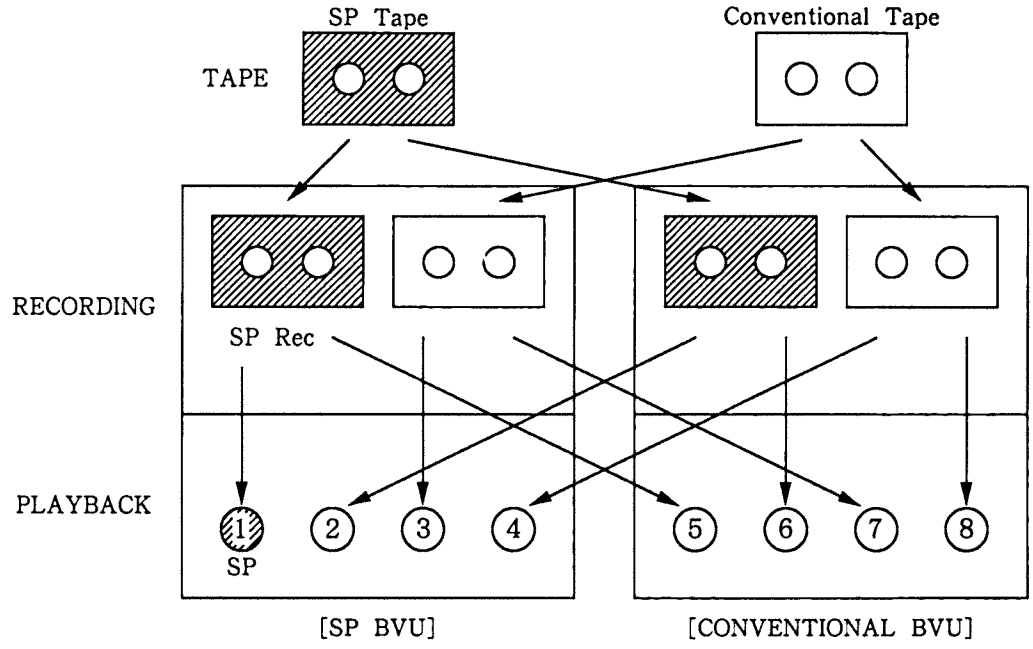


Fig.1-2. SP Tape

1-4. TAPE INTERCHANGEABILITY WITH CONVENTIONAL MODELS

The SP-BVU and conventional BVU have mutual tape interchangeability. If mutual tape interchangeability were ignored, a further improvement in picture quality (resolution) of the video signals would be possible, but this machine gives the highest priority to tape interchangeability.
Fig.1-3 shows the various combinations of tape according to differences in tape used (SP tape or conventional cobalt tape) and VTR used (SP-BVU or conventional BVU).



	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
Y Frequency response (resolution)	＊＊＊				＊＊			
Y ringing	＊＊＊		＊＊		＊＊		＊	
Chroma ringing	＊＊	＊	＊＊	＊	＊		＊	

＊ improved
＊＊ much improved
＊＊＊ very much improved

Fig.1-3. Tape Interchangeability

1-5. IMPROVED VIDEO SIGNAL PICTURE QUALITY

The SP-BVU was designed so that the video picture quality of third-generation dubbed tapes is the same as first-generation tapes dubbed on conventional models.

This unit is capable of recording and playback in the SP mode or conventional mode. When recording, the holes for cassette detection in the SP tape casing are detected by the mechanism switch and the mode is automatically selected. Thus in order to make full use of its performance as an SP model, it is necessary to use SP tape for recording and playback in the SP mode. In the playback mode, the mode is automatically determined by detecting the playback FM carrier frequency. Owing to the above mechanical and electrical automatic detection systems, there be no operational confusion between SP and conventional modes. The SP lamp on the front panel of the BVU-950 indicated whether the VTR is in the SP mode.

1-6. IMPROVED AUDIO SIGNAL SOUND QUALITY

1. New Sendust Head

Frequency response is extended to 50Hz through 15kHz±3dB, and an S/N ratio of better than 52dB when using SP tape.

2. Dolby Type C NR System

This system improves the S/N ratio to approximately 70dB.

3. Dolby Auto-detection circuit

When the Dolby switch is set to "on" and a SP tape is loaded in the REC mode, the machine is placed into the Dolby recording mode. During Dolby recording, the Dolby pilot tone signal indicating the Dolby recording mode is recorded on the audio channel. The pilot tone signal of 1/2 CTL (15Hz for NTSC and 12.5Hz for PAL) is generated by dividing the CTL signal.

In the PB mode, this pilot signal is automatically detected after being synchronized with the playback CTL signal to automatically activate the Dolby circuit for playback. The green lamp on the control panel indicates whether Dolby NR is ON or OFF.

Audio recording equalizer is automatically set whether the tape used for recording is SP tape or conventional tape.

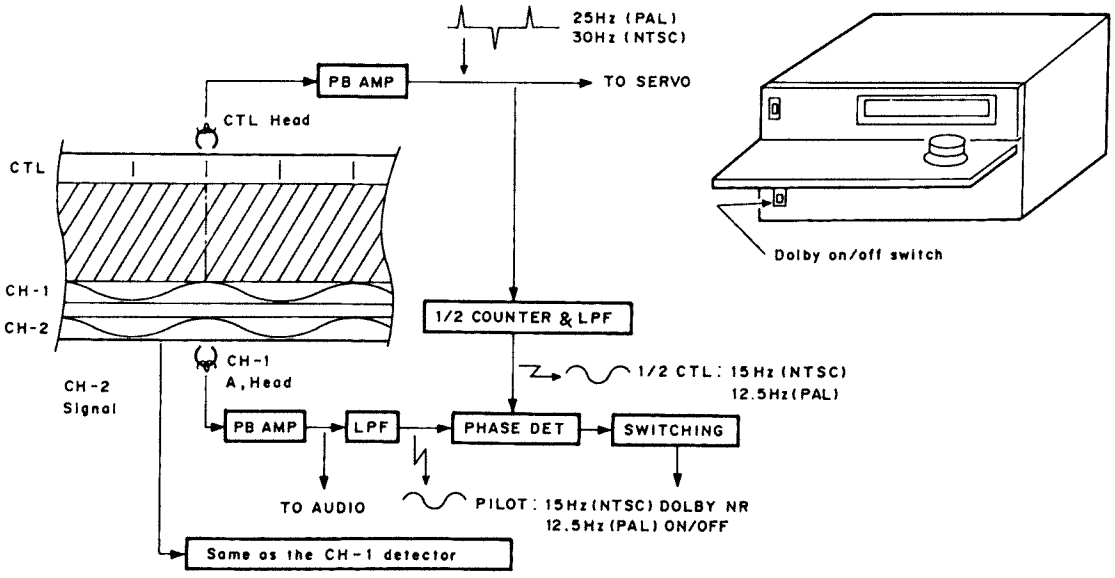


Fig.1-4. Dolby Auto-detection Circuit

1-7. IMPROVEMENT IN AUDIO EDITING

Recording timing of the audio and video are controlled with an exclusive microcomputer. Therefore, the audio erase head is switched ON / OFF approximately three frames prior to the in-point and out-point of the audio signal for smooth starting and stopping during audio insert editing.

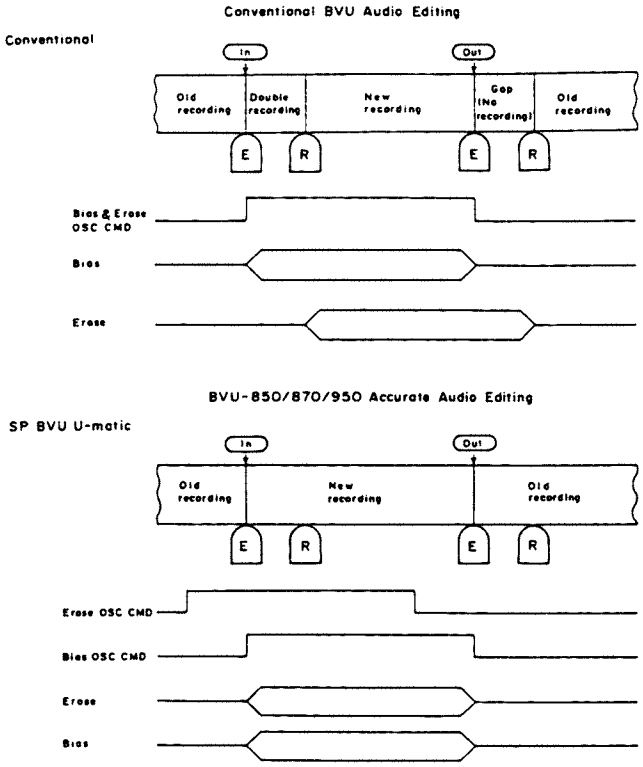


Fig.1-5. Conventional BVU Audio Editing

1-8. PLUG-IN TBC

The plug-in type time base collector BKU-901 is available as an optional accessary. The BKU-901 contains TBC functions and a secondary beat canceller circuit. Remote control of the processor section after time base correction is made possible by using the supplied remote controller BVR-55.

1-9. PLUG-IN TIME CODE

The plug-in type time code generator/reader BKU-905 is available as an optional accessary. The BKU-905 allows presetting of the generator and slave locking to an external generator in addition to the time code kit BK-806 for the previous BVU-800 Series. Characters corresponding to the time code data can be superimposed over the video signal. In addition, the superimposed video signal can be recorded or output from the MONITOR OUT terminal during playing back.

1-10. REDUCTION IN SIZE

The BVU-800 series has a six span size but this model has been reduced to a five span size, the same as type-5 series VTRs. Thus when there is a type-5 VTR installed in the system console, it can be replaced with this machine with the plug-in TBC and the plug-in time code added.

1-11. MICROCOMPUTER SERVO CONTROL

In the previous BVU-800 series, the drum and capstan servo systems were controlled by our company's IC (CX194) for digital servo. This machine uses an 8-bit (16-bit processing) single chip microcomputer which permits a simplification in hardware and stable operation in relation to changes over time and changes in the working environment. The tape tension is electrically servo controlled by a tension detector, rather than through adoption of the mechanical tension servo by tension regulator used in the BVU-800 series. Skew control is also electrical.

1-12. 24-PIN PARALLEL INTERFACE

This machine is equipped with a 9-pin interface as the external interface. For this machine, the 36-pin interface available with the previous BVU-800 series has been abandoned and replaced with a 24-pin amphenol-type interface connector. The 24-pin connector uses parallel signals for interfacing, and as the signal format is opened, the users can use this for their own interface applications.

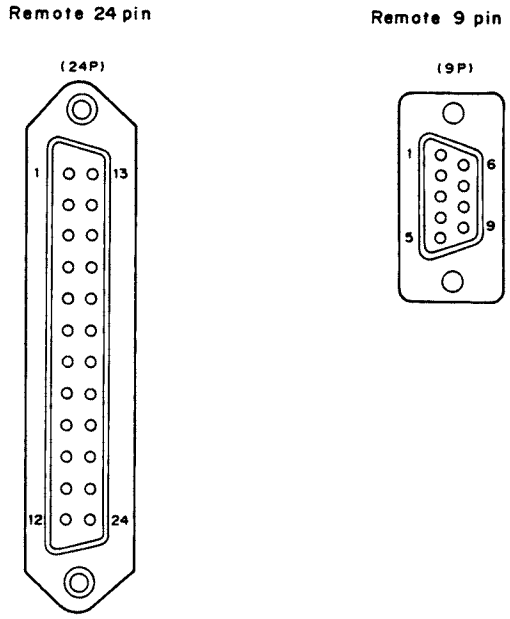


Fig.1-6. Interface

1-13. DIAL MENU

In the previous BVU-800 Series, setting such as the mode for system controller section, etc., were made using the DIP switches located on the board. In this machine, all of this data is stored in non-volatile memory (E^2PROM) which can use semipermanently and the data can be changed according to the front panel switches and jog dial.

1-14. DIGITAL HOURS METER

The previous BVU-800 Series used a mercury hours meter. This machine, however, has two digital hours meters using the internal counters of the microcomputer. One digital hours meter measures the time while the power is supplied to the VTR, and another meter measures the time while the video head is in contact with the tape, and the drum is rotating. In other words, they measure the amount of times the VTR is used and the video heads are used.

1-15. SELF-DIAGNOSIS FUNCTIONS

The ROM on the system control board contains a program for self-diagnosis which allows the data input /output to the various microcomputers to be output from the VTR monitor output terminal as character signal. This permits malfunction analysis when trouble occurs.

1-16. EDITING FUNCTIONS

This machine takes ease of operation during editing into consideration and allows tape transport in the up to ±10 times search mode, FF mode, and REW mode, even while the tape is threaded. This reduces the time required to find the edit point. With the previous BVU-800 series, the tape speed in the FF and REW modes varied according to the diameter of the tape wound on the reel. With this machine, however, the tape is wound with a constant speed to allow the tape to be fast forwarded in approximately 3 minutes and to allow the tape to be rewound in approximately 2 minutes and 30 seconds. The time required to fast forward a tape with the BVU-800 series is approximately 4 minutes. In the shuttle mode of this machine, the playback speed can be altered in nine stages in both the forward and reverse directions. Color playback is possible at speeds up to ±5 times and monochrome playback at ±10 times.

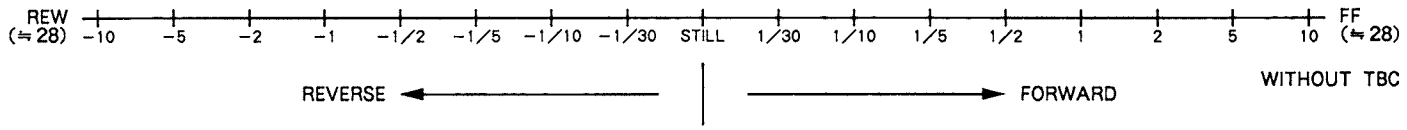


Fig.1-7

1-17. HIGH RELIABILITY MECHANISM

1. Photointerrupter and Illumination LED

In order to ensure high reliability, a photointerrupter consisting of the LED and photosensor is used instead of the micro switches and relays.

Previously, the most frequent reason for service calls was to replace a blown VTR lamp. This machine uses LED for display in the key panel section, illumination of meters, illumination within cassette compartment, etc., greatly improving reliability.

2. DC Motor

This machine uses a total of six DC motors. A brushless motor is used for capstan motor.

3. Tape Tension Detector

The tape tension is detected by separate tension detectors using CdS elements on the T (take-up) and S (supply) sides. The detected tape tension is supplied to the microcomputer for the servo to control rotation of the reel motor and to provide stable tape tension in each mode.

1-18. AUTOMATIC EDITING FUNCTIONS

This machine is equipped with fully automatic editing functions which permit automatic editing. When two BVU-950 units are connected, editing can be automatically performed. The built-in editing functions are: AUTO EDIT, PREVIEW, REVIEW, ENTRY IN/OUT, TRIM, PREROLL, ASSEMBLE, INSERT, etc. Moreover, when the editor BVE-900 is connected, various editing functions can be obtained.

1-19. HIGH-EDITING PRECISION

In the auto-edit mode, the pinch roller is always engaged to the capstan so that ±0 frames editing precision can be obtained by using the reference signal in the CTL editing.

In the STILL mode, the guard band noises are positioned in the top and bottom of the screen by the stop servo circuit.

SECTION 2
VIDEO SYSTEM

2-1. OUTLINE

In order to make the video system more compact while maintaining its high performance, circuit improvements have been made and new parts have been selected, as follows :

a. Circuit Improvements
Y/C separator, RF circuit, noise canceller, etc.

b. Parts Selection
Modular design, filters, variable resistors, etc.

c. Printed Boards
A total of 9 boards including four 4-layer boards that are used in BVU-850, have been concentrated in two 2-layer boards and one single-sided board.

d. Optional Board
A secondary beat canceller circuit, etc. have been transferred to the optional plug-in TBC board. Thus, this unit can be given the same video features of the BVU-850 by attaching to it the plug-in TBC.

2-2. OUTLINE OF MD-44 BOARD

This board consists of the following Y/C signal recording circuits. Its differences with the BVU-850 are shown below.

- Y/C separator with vertical and horizontal correlators
  The BVU-850 uses a glass type of 1H delay line for vertical correlation, however, the BVU-950 uses a CCD type.
- Character insertion circuit
  Not included in the BVU-850.
- AGC amplifier
- Nonlinear preemphasis circuit
- Preemphasis/white & dark clip
- FM modulator
- Record HF circuit
  The pulse phase of RF signal is shifted in this circuit.
- Sync separator
- ACC amplifier
- Frequency converter circuit (AFC/APC)
- Low-frequency range booster

2-3. MD-44 BOARD

2-3-1. Character Insert Circuit

This circuit inserts the characters such as time code information, etc., in the video signal. The signal input to the LINE VIDEO connector on the rear panel is fed into this circuit. Signals inserted into the video signal are recorded on tape in the record mode. Operation of this circuit can be turned on/off by the character ON/OFF switch at the bottom of the front panel. The LINE VIDEO signal input to pin 1 of CN610 on the MD-44 board is fed into the buffers Q1 and Q4. Q4 output is input to pin 5 of the switcher IC1 as background video level which is half level of input video signal reference to the pedestal level. The pedestal voltage of the video signal sent from buffer Q1 is detected by the sample and hold circuit consisted of Q2, C3 and IC16. The characters are inserted by means of Q6 and IC1.
The AGC error voltage that is adjusted by RV29, is output from pin 7 of IC17 so that the character level becomes stable against the level fluctuation of the input video signal. The video signal processed at the character insert circuit is fed into an LPF consisting of L3, C8 and C9. This LPF operates as a CCD prefilter, it limits the bandwidth of CCD, and is preventing the foldover noise of the CCD.

2-3-2. Delay Circuit (Vertical Correlator)

This unit uses a CCD as 1H and 2H delay line. Output of the buffer Q8 is divided into the 0H delay circuit and the 1H/2H delay circuit.
The 1H delay circuit consists of Q11 through Q16, Q93, IC3, IC4, FL2, etc. Signal is delayed approximately 100nsec by Q11 and Q12, then it is fed into IC3 via the buffer Q39. The RV1 is used for adjusting CCD bias so as to obtain an optimum CCD output linearity. After passing through RV1, the signal is input to the CCD inside the IC via pin 8 of IC3, and delayed 1H by means of a 680 bits shift register. A 3fsc (10.7MHz) signal generated by Q42, FL5, FL6 and IC13 is used as clock signal for the CCD. Therefore, delay amount of the CCD itself is 680/3fsc. The fsc of the chroma system is used for the 3fsc. This fsc is input to the ceramic filter composed of FL5 and FL6 to extract its triple harmonic. The obtained 3fsc is boosted at IC13, passes through the buffer Q43 and input as clock signal for the CCD composed of IC3 and IC4.
The signal delayed 1H by IC3 is fed into an LPF with a cutoff frequency of 4.5MHz (FL2) via the buffer Q13. The CCD output contains a 10.7MHz clock component which is suppressed at FL2. In order to take vertical correlation, level and phase of the three signal kinds (0H, 1H and 2H) should be exactly matched. The delay amount is precisely adjusted to 1H by Q14, C35 and RV2. From the 1H delay signal obtained in this way, the chroma signal is extracted by the HPF consisting of C37, R48 and R49. Level of this signal is adjusted by RV3, then it is input to the IC7 correlator after being boosted 20dB at IC4.
The 2H delay block configuration is similar to that of the 1H delay block. The 0H block also includes an LPF (FL1), so that the signal matches the characteristic with 1H and 2H signals. The signal whose vertical cross-color has been suppressed by the vertical correlator is delayed 140nsec and 280nsec by DL1, then input to pins 6 and 4 of IC7 for horizontal correlation processing. The horizontal correlator suppresses cross-color which cannot be removed by the vertical correlator. After horizontal correlation processing, the chroma signal is output from pin 12 of IC7, delayed at Q24 and output to the edge compensator.

2-3-3. Y Signal Separator Circuit

The Y signal is generated by subtracting the chroma signal from the composite video signal. At the vertical correlator, the 1H signal is treated as the main signal among 0H, 1H and 2H signals. Therefore, the chroma signal output from the correlator is delayed 1H from the input signal, so the signal delayed 1H by the IC3 CCD is used as composite signal for Y signal extraction. An amount of the Q15 buffer output equivalent to the delay produced by DL1, DL2, etc. is compensated at DL5, Q33 and RV9, and the chroma signal portion fed via TP6 and RV11 is subtracted. At this point, level and phase of the 1H and 2H signals must match perfectly under their respective temperature characteristics. Otherwise, a chroma signal component will remain in the Y signal. The carrier leak cancel circuit of the next stage is designed to remove this residual chroma signal component.

2-3-4. Carrier Leak Cancel Circuit

The Y signal containing carrier leak components is divided just before R101, one path is amplified by Q31, its leak component is roughly removed by the R86 and L16 high-pass filter, and the high level components of Y signal is removed by the limiter consisting of D21 and D22. The leak component is input to the IC11 horizontal correlator via IC10, and the chroma component carrier leak is extracted. Phase of the Y signal containing an original carrier leak component is matched to that of the extracted leak component, and the carrier leak is then canceled by Q36 and Q37. IC9, IC15, Q27 and Q32 integrate a carrier leak component detector circuit which cancels just the parts where carrier leak is present. The Y signal is amplified by the differential amplifier consisting of Q38 and Q40, then output via the IC201 video switcher. The DUB Y signal is input to pin 3 of IC201, so when pin 6 turns "low" the DUB Y signal is selected. This selection is controlled by the signal input to pin 3 of CN612, which turns "low" in the DUB mode (it is "high" during the LINE mode). The selected Y signal is input to pin 13 of IC204 (AGC amplifier) via the Q45 buffer. After being processed at the AGC amplifier, the Y signal is output from pin 15 of IC204 and divided into three: DUB/LINE (SP) /LINE (CONV). The Y signal for DUB passes through the delay circuit consisting of Q51 and Q52, then it is input to pin 19 of IC204. The remaining two LINE outputs are fed into their respective SP and conventional mode LPFs (FL202, FL201) in order to limit Y signal bandwidth.

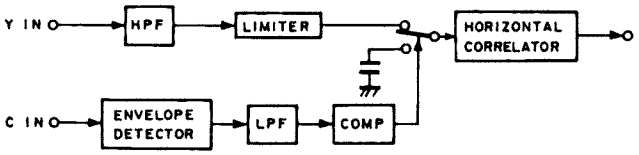


Fig.2-1. Carrier Leak Cancel Circuit

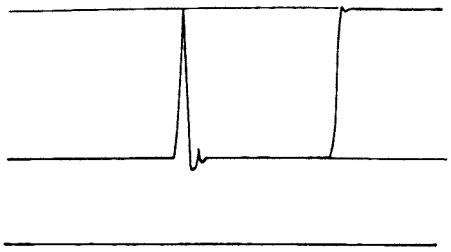
2-3-5. Edge Compensator

Cross-color caused by Y signal components leak in the chroma signal is suppressed at the horizontal correlator, but the chroma signal edge component is also lost. The edge compensation circuit is designed to compensate for this.

The horizontal correlator output from pin 12 of IC7 is delayed at Q24 and input to the IC8 edge compensator. The input signal is amplified for approx. 7dB at IC8, it is output from pin 4, and delayed for 140nsec and 280nsec at DL2. Delayed signal is input to pins 7 and 5 of IC8, reaching the edge compensation correlator inside IC8 . After compensation, the signal is output from pin 12, and 2fsc secondary distortion introduced by the correlator is removed by the LPF. The chroma signal is then output from pin 2 of IC8, and fed into the IC401 ACC amplifier in the MD-44 board via TP6.

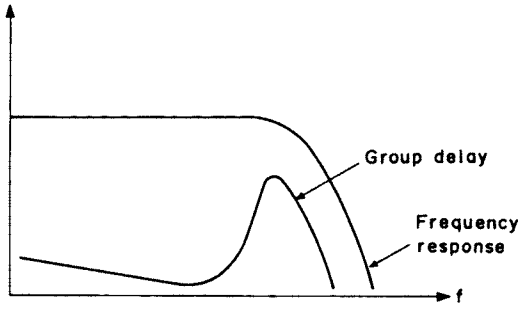
2-4. Y SIGNAL SYSTEM

If Y signal processing is performed just by the LPF (FL201, FL202), passing bandwidth high-range phase will be delayed, causing the overshoot shown in Fig. 2-2. This appears as ringing on the picture.



2T-PULSE/2T-BAR SIGNALS

Fig.2-2 (a). Waveform Characteristics



LPF TRANSFER FUNCTION

Fig.2-2 (b). Transmission Characteristics

2-4-1. Phase Equalizer

Y signal waveform is deteriorated each time dubbing is performed. This circuit minimizes phase variation. Phase equalization is performed by adding the group delay shown as a broken line in Fig.2-3 to the input Y signal group delay (full line) and flatting the total group delay characteristic. Fig.2-4 shows the output waveform when a 2T pulse signal and a color bar signal are input.

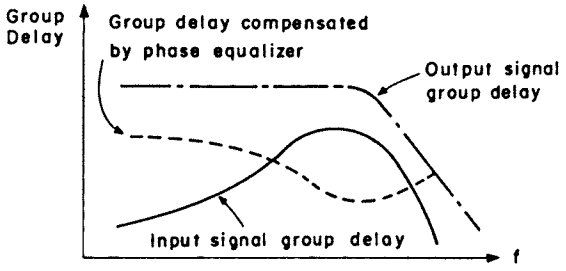
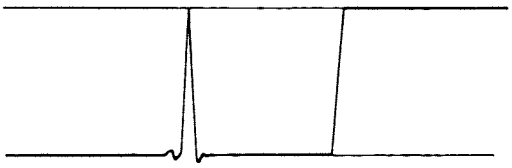
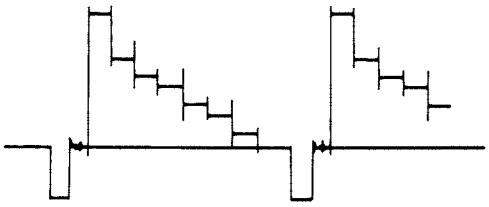


Fig.2-3. Group Delay



2T-PULSE/2T-BAR SIGNALS

Fig.2-4 (a). Output Waveform of 2T Pulse Signal



75% COLOR BARS

Fig.2-4 (b). Output Waveform of Color Bar Signal

2-4-2. AGC Amplifier

Y signals whose phase has been equalized at Q47/Q104 and Q49/Q50 are switched at IC202 and input to pin 17 of IC204 video amplifier. The output from pin 21 of IC204 is input to pin 22 of IC204, sync-separated and output from pin 24. This output is input to pin 1 of IC204, mixed to the Y signal and input to the sync AGC detector in the next stage. Output of the AGC detector is extracted from pin 3, and its error voltage is integrated at the filter composed of R231, C155, C153 and R238. The error voltage is input to pin 16 of IC204 via RV23 and boosted by the DC amplifier. This voltage controls the AGC amplifier. RV23 is used for adjusting the deviation of AGC level control. The D7 cathode is connected to the external video level control terminal. In the manual mode, video level adjustment is possible by varying the DC voltage using the front panel video control potentiometer.

2-4-3. Non-linear Preemphasis and Feedback Preemphasis

The Y signal passes through the Q53 buffer, then it goes into IC203. Its low-level high-frequency component is then output to TP204. This high-frequency component and original Y signal are mixed by R176 and R177 and input to pin 4 (TP205) of IC204 via Q56 and then clamped. Q55 is switched by a "high" signal during the DUB mode to mute the output of IC203. The signal passing through the non-linear preemphasis circuit is fed to the feedback preemphasis circuit composed of Q60 and Q62 to Q65 and Q110 to Q118 and Q120. The output signal from the buffer Q56 is input to the differential amplifier composed of Q60 and Q62 to Q65. The signal input to the base of Q60 is output from the collector of Q64 in the same phase, and fed to the FM modulator via the buffer Q112 and amplifier Q114. The output from Q112 is fed back to the base of Q65 via the de-emphasis circuit composed of C147, C148, R193 and R194 as a feedback loop of differential amplifier.
As described above, de-emphasis circuit has been provided at the feedback circuit of the feedback loop, the output signal from Q112 is preemphasised.
In the loop, white clip circuit composed of Q120 and Q3, dark clip circuit composed of Q110 and Q111 are provided in order to clip the white and dark peak-over components.

2-4-4. Modulator

In the CONV mode, the residual subcarrier component in the Y signal is removed by the trap LV1 and C334 connected to the emitter of Q114, then input to the FM modulator inside the IC204. Sync-tip carrier frequency adjustment of the SP mode is performed by RV19, and sync-tip carrier frequency adjustment of the conventional mode by RV20. Incidentally, Q69 is on in the SP mode. RV18 performs balance adjustment of the FM modulator, it minimizes secondary distortion at the modulator. The signal is output from pin 10 (TP211) of the FM modulator, fed into pin 14 of IC205 and input to the record HF circuit.

2-4-5. Record HF Circuit

RV21 is used for balance adjustment of the record HF circuit, and is adjusted so as to minimize the second harmonic of the FM signal that is output from pin 3 of IC205. The Y-FM signal output to TP212 is divided into two branches: FL203 (conventional mode) and FL204 (SP mode). Y signal record current adjustment for the conventional mode is performed by RV22. The Y signal in the conventional mode is input to pin 5 of IC207 and the Y signal in the SP mode is input to pin 3 of IC207 and they are output from pin 1. Control signal of IC207 is phase-inverted by Q70. The selected signal is output to the RP board via pin 1 of CN607. In the EE mode, it is output to the DM board via pin 1 of CN606.
The Y-AGC error signal is input to pin 6 of IC206, then fed to the video meter. RV25 is adjusted so that the video meter displays the reference point when a 1Vp-p video signal is input.
The playback RF signal is input to pin 4, and tracking meter level is adjusted by RV24. Selection of REC/EE mode and playback mode is controlled by the DC voltage input to pin 3. The REC/EE mode is selected at "high" level, and the playback mode at "low" level. The playback RF signal from the DM board is input via pin 3 of CN606 and TP213 and fed into pin 14 of IC206. This input signal is amplified and output from pins 10 and 8. The signal from pin 10 is output from pin 1 of CN612 via TP214 as an off-tape RF signal, then fed into the external TBC as a DOC detection signal. Pin 8 output is sent to the DM-54 board from pin 1 of CN609 as an RF envelope signal.

2-5. RECORD ACC/APC/AFC CIRCUITS

After Y/C separation, the chroma signal is input to the ACC circuit IC401 via TP408 on the MD-44 board, then output from pin 3 (TP404). The signal input to pin 2 of IC401 is input to the frequency converter circuit and the addition and the subtraction frequency components with the 4.27MHz signal input to pin 1 are output from pin 24.
At LPF (FL401), only the low frequency component (688kHz) of signals converted to 4.27MHz and 3.58MHz is extracted and input to Q82. Q82 is a delay circuit for Y/C delay adjustment and output level is adjusted by RV202. DL401 is a delay line for Y/C delay adjustment capable of controlling the delay amount in 50nsec units. The signal input to pin 3 of IC404 and the DUB chroma signal input to pin 5 are selected according to pin 6 control voltage and output from pin 1 (the control voltage at pin 6 is "high" in the DUB mode). The DUB chroma signal fed to the DUB connector is input to delay circuit Q76 via pin 3 of CN611 on the MD-44 board. The delayed signal is then fed to pin 5 of IC404. The output from pin 1 (TP407) of IC404 is divided in two branches, one is fed to the low frequency booster IC405, and the processed chroma signal is then output to the RP-30 board via pin 3 of CN307. The other branch is selected by the switcher Q84, and the EE mode chroma signal is output to the DM-54 board via pin 6 of CN606. Incidentally, the switcher Q84 is turned on by a "low" level signal.

2-5-1. AFC Loop

The Y signal is input to pin 22 of IC402 for sync separation. The sync-separated output is input to the half-H killer circuit in the next stage, EQ pulse is removed, and it is converted into an H sync signal. After EQ pulse removal, the H sync is input to the sample and hold circuit as a sampling pulse. The AFC loop consists of the VCO, the countdown circuit (NTSC : f/350), the slope circuit and the sample & hold circuit inside the IC402. In order to lock the VCO output to the sync signal separated from the input video signal, sampling is performed by sync pulses. The ramp waveform in the sampling can be monitored at TP401, and phase error voltage can be monitored at TP402. Oscillating frequency of the VCO is 350×fH for the NTSC system. The operating point of the AFC loop can be adjusted by RV303. VCO output is first divided by 8, then input to the frequency converter circuit. Therefore, the 4.27MHz signal obtained after frequency conversion is synchronized with the H sync of the input video signal. The H sync signal is delayed by L51, C267 and C268, and burst-flag pulses are generated. R305 and C265 are LPF, along with Q86, to mute the burst flag pulses within the V blanking period. Burst flag pulses from TP409 are input to pin 16 of IC401 and fed to the burst gate circuit. The burst gate circuit output is fed to the APC and ACC detectors, and used as a switching pulse for error detection within the burst period.

2-5-2. APC Loop

The chroma signal output from pin 2 (TP404) of IC401 is input to pin 12 of chroma amplifier IC401. The output of the chroma amplifier is input to the APC detector, the chroma signal burst phase is compared with the 3.58MHz phase generated by the VCO, and the detected phase error voltage is output from pin 14, thus oscillation frequency of the VCO (composed of X1 and D18) is controlled. The output is delivered through pin 19 via the reference oscillator IC401, then it is input to pin 15 of IC401 via the reference phase shift circuit (L49, C255, R296). The other branch is fed back to the VCO loop via T1. In this way, the 3.58MHz signal locked to the subcarrier phase of the input chroma signal is output from pin 19 of IC401. T1 is used for tuning the VCO center frequency. The operating point of the APC loop is adjusted by RV304, so that the frequency is adjusted for 3.579545MHz. The reference oscillator output is also fed to the ACC detector, where peak detection at the burst portion of the input chroma signal is performed. The error voltage obtained as a result of peak detection is fed to the DC amplifier, and this DC voltage is used to control the ACC amplifier. When output of the DC amplifier drops below a determined level, the ACK detector is activated and muting is applied to the frequency converter circuit, the chroma amplifier, etc. The 3.58MHz signal locked to the subcarrier output from pin 19 of IC401 is input to pin 7 of IC401, frequency-converted with the 688kHz signal locked to the Y signal fH, then output from pin 5 to the BPF (FL402) as an addition and subtraction signals. At the BPF, only the added component (3.58MHz+688kHz= 4.27MHz) is extracted. This 4.27MHz signal is synchronized with the input video signal fH, its level is adjusted by RV301, and it is input to pin 1 of IC401 via the amplifier Q87. The 3.58MHz chroma signal is input to pin 2 of IC401. The 4.27MHz signal input to pin 1 is frequency-converted, then output from pin 24 as an addition and subtraction signals. The output signal is fed to the LPF (FL401), where only the subtracted component (4.27MHz−3.58MHz =688kHz) is extracted and input to the chroma amplifier Q82. The 4.27MHz carrier signal is output to the RP-30 board from pin 5 of CN607 as a rotary erase signal, via the buffer Q809.

2-6. RP-30 BOARD

This board consists of the record amplifier, playback head amplifier and rotary erase amplifier.

2-6-1. Record Amplifier

The Y-RF signal in the record mode is input to pin 6 of CN703, and the recording level in the SP mode is adjusted by RV2. The chroma RF signal is input to pin 4 of CN703. Recording level of the chroma signal is adjusted by RV1 and signals are mixed inside IC1. The Y/C mixed signal is amplified by record amplifiers IC2 and IC5, its frequency characteristic is adjusted by RV3 and RV5, and it is fed to the head.

2-6-2. Playback Amplifier

The playback head amplifier, composed of IC3 and IC6, has a almost flat frequency response ranging from low to high areas. RV4 and RV6 are resistors used to dump the resonance frequency of the head, and they are adjusted so that the 1MHz through 9MHz range becomes almost flat. Therefore, the frequency characteristics of the electromagnetic conversion system is output as the head amplifier output.

2-7. DM-54 BOARD

2-7-1. Outline

This board consists of Y signal and C signal playback circuits. Follows an explanation of its main blocks, its outline and its differences with the BVU-850.

- Playback RF amplifier :
  In this machine, midrange compensation is performed by resonant circuit, however, aperture compensation is used in the BVU-850.
- Playback HF Circuit :
  Same circuit configuration as in the BVU-850.
- Demodulator :
  Same circuit configuration as in the BVU-850.
- Dropout Compensator :
  A CCD (CXL5001P) is used as 1H delay line, and the clamp circuit for 1H delay signal is adopted.
- Noise Canceller :
  It has been simplified, consisting of just one hybrid IC.
- Character Insert Circuit :
  A circuit to insert time code and other characters to the monitor output has been added.
- SP/conventional Mode Detector :
  A circuit allowing playback of tapes containing parts recorded in two modes has been added to the BVU-850 mode detector circuit.
- DG compensator
  The same characteristic as that in BVU-850 has been realized simplifying the circuit.
- Selection of reference subcarrier
  During EE mode, the chroma output is always locked to the input signal that waveform on the vectorscope locks.
  The followings are the selection of reference subcarrier signal during palyback.
  Normal playback : Internal 3.58MHz oscillator
  Internal TBC mode : Return SC signal sent from INT TBC
  External TBC mode : Return SC signal sent from EXT TBC

2-7-2. Playback Amplifier

The playback CH-A and CH-B signals are fed from the RP-30 board to pins 28B and 30B of CN103 on the DM-54 board, then input to pins 24 and 23 of RF amplifier IC1.
In the BVU-850, midrange frequency response compensation is performed by an aperture compensator. This circuit compensates the high frequency response of RF signal by means of a cosine curve, and prevents midrange tuning dispersion at CH-A and CH-B heads. This aperture compensator has also the effect of reducing phase distortion.
In this machine, the LC midrange tuning system is used instead of the aperture compensator. By changing parameters of peripheral circuits, a performance equal to that of the aperture compensator can be achieved.
8MHz is tuned by L3/C6 and L4/C7, which are respectively connected to pin 21 and 20 of IC1, then dumping is adjusted by RV2 and RV3. CH-A and CH-B RF signals are switched by the RF switching pulse input to pin 18 of IC1, then Y-RF and C-RF signals are respectively mixed in by RV6 and RV4. The Y-RF signal balanced by RV6 comes through the buffer Q3. Q6 is turned on in the normal playback mode, and C9/C10 are connected in parallel. In the still mode, however, Q6 is turned off to reduce the over-modulation around the guard-band portion. High frequency component of this signal is attenuated by an LPF composed of L7, C13, C14 and C15 so that the occurrence of over-modulation is reduced and then input to the buffer Q8. The Y-RF signal is level adjusted by RV5, then it is input to the switcher IC2. The playback Y-RF signal is input to pin 3 of IC2, and the EE mode Y-RF signal is input to pin 5. Both signals are switched by the control voltage at pin 6. The "EE 12V (H)" signal is input to pin 6 of IC2, causing the signal fed to pin 5 in the EE mode to be output through pin 1 (TP3). Output of IC2 is input to pin 15 of IC1 via the high-pass filter FL1 in the SP mode, and to pin 14 of IC1 via the high-pass filter FL2 in the conventional mode.

2-7-3. Playback HF Circuit

This circuit compensates high frequency response of RF signal by means of a cosine curve, thus preventing overmodulation. High frequency response compensation can be performed by setting the cosine curve peak to a specific frequency. Also, as group delay for this circuit is constant, no RF phase distortion is generated. Overmodulation occurs at around 10MHz, so frequency response is compensated so that the gain peak is around 10MHz. Peak frequency is determined by the delay amount of the delay line.
In the SP mode, a "high" level control voltage is input to pin 12 of IC1. IC1 has a built-in limiter and output is delivered through pin 9, then divided in two branches via the buffer Q13. This limiter output can be monitored at TP5. One branch is input to the HF circuit, and the other one is input as Y-RF output to the MD-44 board from pin 12B of CN103, via the buffer Q14.
Pin 13 of IC3 is the input terminal of the HF circuit, and frequency response of the Y-RF signal is compensated for. The actual playback HF circuit is composed of IC3 (BX1140L), DL1, DL2 and Q16. The delay lines DL1 and DL2 respectively inserted between pins 9/8 and 8/3 of IC3 determine the frequency response compensation amount. RV8 performs carrier balance adjustment as DC balance of IC3 is changed. Q16 is turned on in the conventional mode, and first-stage HF circuit is turned off to boost the low frequency of RF signal properly. The playback HF circuit output is input to pin 1 of IC4, then input to the demodulator via the limiter. The linearity of the demodulator is determined by the capacitor (C38) connected to pins 24 and 23 of IC4. The Y signal output from pin 21 of IC4 is deemphasized by R50, R51, C40 and C41, and its second harmonic is removed by the low-pass filter FL3. In the conventional mode, it passes through the low-pass filter FL4. The signal input to pin 19 of IC4 is output from pin 16 via the video amplifier, then input to pin 1 of IC6. If time code has been recorded, the noise component modulated by the time code during V blanking period, is muted by Q37. This signal is amplified again by IC6, then output from pin 6. Incidentally, output waveform can be monitored at TP9. The output is divided in two branches and input to the switcher IC4. The signal at pin 7 is for the SP mode, and its level can be adjusted by RV11. The conventional mode signal is input to pin 12, phase equalization is performed by Q22, then it is input to the low-pass filter FL4. CV1 is used for adjusting the frequency response of the playback Y signal in the conventional mode. RV12 performs phase equalization of IC7 in the current

mode. The signal whose level has been adjusted by RV16 is input to pin 12 of IC4, switched by the control voltage input to pin 11 and output to pin 4. SP mode phase equalization is performed by Q23 and IC8, and the signal is output from pin 3 (TP14) of IC8. CV2 is used for SP mode playback Y signal frequency response adjustment, and LV101 for phase equalization.

2-8. DROPOUT COMPENSATOR

This machine uses the method of replacing the dropout portion with the 1H before video signal (video dropout compensator). A Sony CCD is used as Y signal 1H delay line. Incidentally, a separate clamping circuit is used when replacing the dropout portion with a signal delayed 1H.

IC10 is a dropout compensation switcher. The Y signal from the phase equalizer is input to pin 3 of IC10, and the 1H delayed Y signal is input to pin 5. The output from pin 1 of IC10 is input to pin 8 of IC202 (CCD), and the 1H delayed Y signal is output from pin 5 of IC202. The 3fsc signal generated from the 3.58MHz of the playback chroma signal is used as clock pulse for IC202 (CCD). This 3fsc is produced at the PLL circuit IC201. The output from pin 5 of IC202 is fed to FL201, the CCD clock component is removed, and it is input to IC204 in the next stage for amplifying. RV201 is used for adjusting the level of the 1H delayed Y signal. Q27 is for clamping of the 1H delayed Y signal. Y signal on the main line is sampled by Q25 and then held with C27, so that the pedestal voltage is detected. The 1H delayed Y signal is clamped by this output signal, thus equalizing APL between both inputs of IC10.

The dropout pulse detector is built into IC251. The RF envelope signal generated at IC1 is output from pin 7 and input to the dropout detector inside the IC via pin 9 of IC251 for generating the dropout pulse. RV251 is used for adjusting the dropout detection sensitivity. The dropout detector output passes through the two branches of the muting circuit inside the IC251, then it is output from pins 1 and 4, respectively. The output from pin 1 is fed to the TBC dropout terminal (it is muted when EE+12V is "high" or the servo is not locked). The output from pin 4 is input to Q30 via TP251, and it is used as the VTR internal dropout control pulse. The DOC circuit output is input to Q34 via the delay line DL4 and the amplifier IC11, and phase equalization is performed for the noise canceller in the next stage.

2-9. NOISE CANCELLER

Fig.2-5 shows a block diagram of this circuit. It is composed of IC12 and Q42.

A non-linear emphasis circuit is built into the feedback loop of this circuit. At the playback stage, noise reduction is performed for the amount of emphasis added when recording. Also the BVU-850 is equipped with this circuit, but the BVU-950, a 3.58MHz tuning circuit has been added to the feedback loop so that the total characteristic of the noise canceller is that minute components at around 3.58MHz are cancelled 20dB against low frequency signal. It is mixed with the chroma signal via the Y buffer IC401. RV402 and RV401 are used for adjusting the mixing level of the Y signal and chroma signal.

The VD signal is input to pin 7 of IC401. This VD signal is added to the Y signal, thus preventing V-sync loss during search. The processed Y signal passes through the output amplifier and it is input to pin 3 of the switcher IC402 from pin 8 of IC401. A signal which received time base compensation by BKU-901 is input to pin 5 of IC402. When the TBC switch is set to on and the plug-in TBC is installed, the signal from pin 5 of the TBC is selected. The signal for VIDEO OUT 1 is driven by IC404 and IC405 (a ±12V voltage is fed to these ICs). In this way, the signal is output as a DC coupled signal, reinforced against sag. Time code and other characters can be inserted into the signals for MONITOR OUT by means of the superimpose circuit composed of Q402 through Q411 and IC403. Pedestal of the switcher IC402 output is clamped by Q409 and Q403, and the level is shifted by Q410 and Q405. The signal at pin 13 of IC403, whose level is low at the character background, is selected by the CHARACTER BACK signal input to pin 15B of CN104. An approx. 5.8Vdc voltage is applied to pin 1 of IC403, pin 1 is selected by the character signal input to pin 16B of CN104, thus inserting the character into the video signal. When no characters are inserted in the video signal, pin 3 of the switcher consisting of pins 3, 4 and 5 of IC403 is selected, and a signal the same as VIDEO OUT 1 is output to MONITOR OUT.

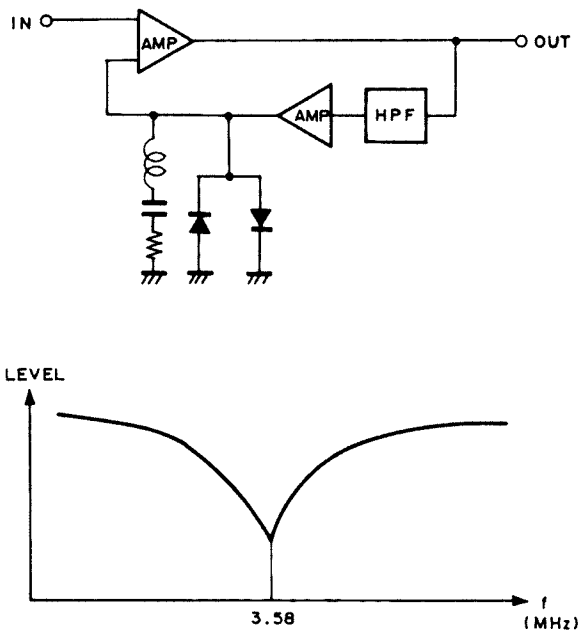


Fig.2-5. Noise Canceller

2-10. SP MODE/CONVENTIONAL MODE DETECTOR

The Y-FM signal spectrum for SP and conventional mode playback is shown in Fig.2-6. The mode can be specified by determining whether the sync-tip carrier (3.8MHz : NTSC) in the conventional mode is present or not.

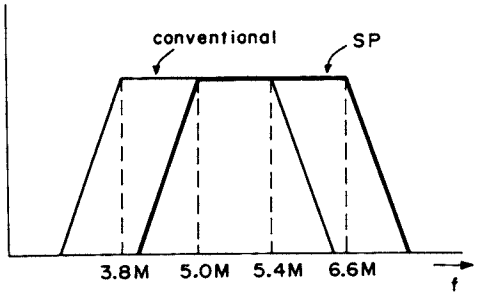


Fig.2-6. Y-FM Signal Spectrum

SP video cassette tapes have holes for SP mode detection. During playback mode, when an SP tape is used and FM carrier frequency in SP mode is detected, the VTR automatically operates in the SP mode. However, if the sync-tip carrier in the conventional mode is detected, the machine will operate in conventional mode even if an SP cassette is inserted. For normal recording, only cassette hole detection is performed before starting to record in the SP mode. The logic control operations above are performed by IC304.

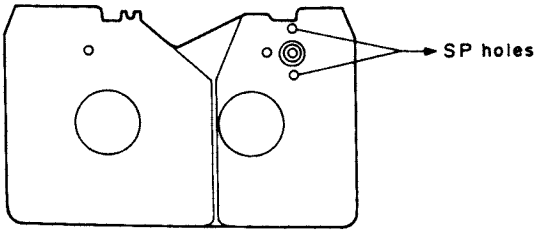


Fig.2-7. SP Tape Detection Hole

IC301, IC302 and IC309 operate as follows. If a tape recorded in the SP format is edited in a VTR such as the BVU-800, both the conventional and SP formats remain on the tape. When such a tape is played back, Y signal carrier is shifted at the point where the signal format has been switched, the demodulated Y signal is DC-shifted, and the playback picture is disturbed. This occurs because the DC shift of the Y signal at the edit point causes malfunction of the sync separation of the monitor. In this machine, mode is detected beforehand at the RF overlap section, so the DC level of the demodulated Y signal can be shifted by the switching pulse timing, thus preventing it from adversely affecting playback. In VTRs using a framing servo, editing starts from the CH-B, so mode detection is performed at the CH-B overlap section. Picture disturbance is prevented by shifting DC level of the demodulated Y signal on the basis of this mode detection signal. A block diagram and the corresponding waveform are shown in Fig.2-8 to 2-11.

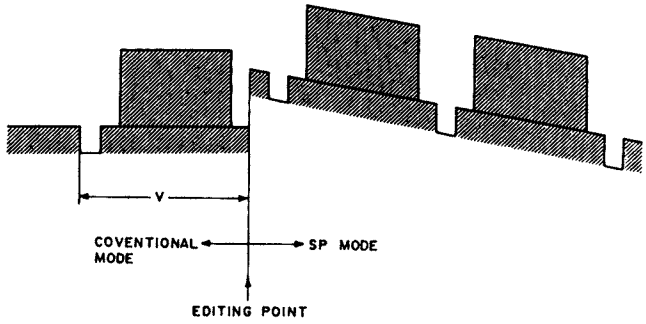


Fig.2-8. Editing Waveform

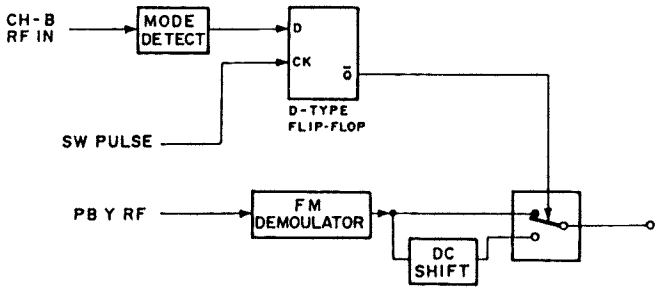


Fig.2-9. Conventional Mode Block Diagram

The CH-B RF signal is input to the amplifier IC301 via the HPF composed of R301 and L302. By means of this HPF, the detection margin between the conventional and SP modes is sufficiently enlarged. The amplified RF signal is set to a constant level by the limiters D301 and D302, then input to the switcher IC302 via Q309. A "high" level signal is input to pin 6 of IC302 during the search or still modes, and when the servo system is not locked. Therefore, during normal playback the RF signal of the CH-B overlap section is output from pin 3 of IC302 through pin 1, its level is adjusted by RV301 and it is input to pin 16 of IC303. The signal is demodulated by IC303 after being tuned to the conventional mode sync-tip carrier (3.8MHz) by LV301. Therefore, a demodulated output waveform whose sync has been tuned can be obtained at TP301.

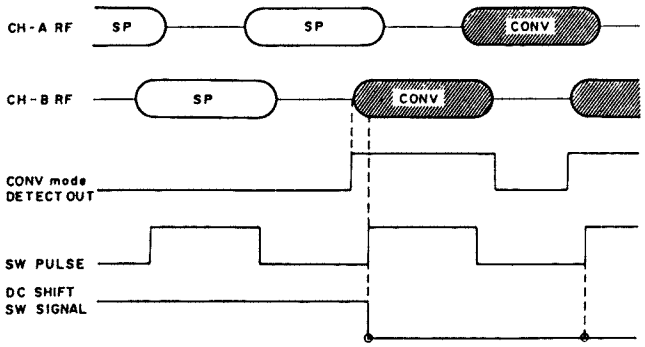


Fig.2-10. Editing Timing Chart

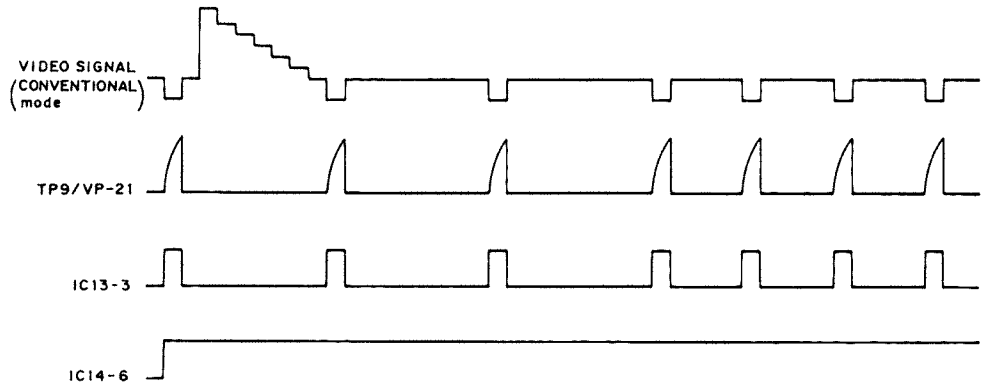


Fig.2-11. Conventional Mode Waveforms for Each Section

The demodulated output is input to the retriggerable monostable multivibrator IC305, and a pulse with approx. 9H width is output. This output pulse is input to pin 11 of IC304, and mode is switched by the rising edge of the switching pulse which is input to pin 1 of IC304 via Q305 during conventional mode playback. During conventional mode playback, pin 12 of switcher IC5 is selected, and a "high" level SP signal is fed from pin 12 of IC5 to pin 7 of IC304. The cassette hole detection DC voltage is input to pin 6 of IC304, becoming "high" when an SP cassette is inserted. Therefore, finally a "high" level signal is output from pin 2 of IC304 during the SP mode. A "high" level signal is input to pin 13 of IC304 via D303 during recording, and the signal from the mode detector circuit is inhibited. In this way, the operation mode of the video system is determined according to the cassette type input to pin 6 of IC304. When search operation is performed using the TBC, there is a possibility that the mode detector circuit will malfunction due to changes in the tape-to-head relative speed. To prevent DC shift malfunction, a "low" level signal is input to D304 from pin 21B of CN103 in search speeds above ×1.2, thus compulsory setting the machine to the cassette detection mode. When the editing point is reached on the monitor screen in other search and still modes, mode is detected by the RF output signal of the playback HF circuit, and switching is performed directly at the DC shift circuit by IC302. Q301 and Q302 are circuits used to increase guard-band detection sensitivity. At the guard band, Q302 goes on and Q301 off, increasing the RF level which is input to pin 5 of IC302. The DC shift circuit consists of IC5 (1/3), Q19 and RV9. The DC voltage determined by RV9 is applied as bias via Q19, thus preventing DC difference between the SP and conventional modes, and further, this circuit does not work in the normal operation, however, it functions when the switch S301 is set to OFF position.

2-11. DG COMPENSATOR

In the low frequency conversion recording system, the chroma signal is superimposed to the FM carrier of the Y signal, so recording is performed at two different frequencies. The bias effect is generated between them, causing DG (differential gain) deterioration. If recording or playback is performed in this condition, the recording or playback Y signal carrier frequency affects playback chroma signal, increasing the chroma level where the white area of the Y level is high as shown in Fig.2-12. DG deterioration is usually considered a result of the influence of amplifier distortion, but as a matter of fact amplifier distortion is almost completely unrelated, being elements originated in electromagnetic conversion processing the most important. Without DG compensation, difference between maximum and minimum levels of the Y signal carrier is approx. 15%, and as stated above DG distortion corresponds to this carrier. At the DG compensator, the Y signal is modulated to the reverse phase to compensate DG distortion.

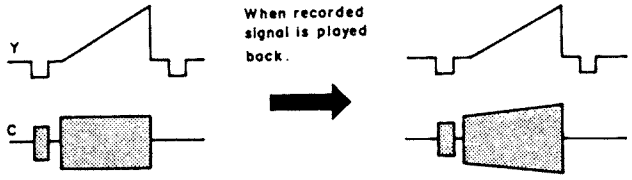


Fig.2-12. Record/Playback of Linearity Signal

2-12. HIGH SPEED ACC

With standard ACC amplifiers, it is not possible to follow up components which are altered by high frequencies within the field. The high speed ACC circuit of this unit detects the error caused within the field by head-to-tape contact irregularity, performs AM modulation and multiplies the error component into the main line, decreasing the amplitude fluctuation of chroma signal due to contact irregularity.

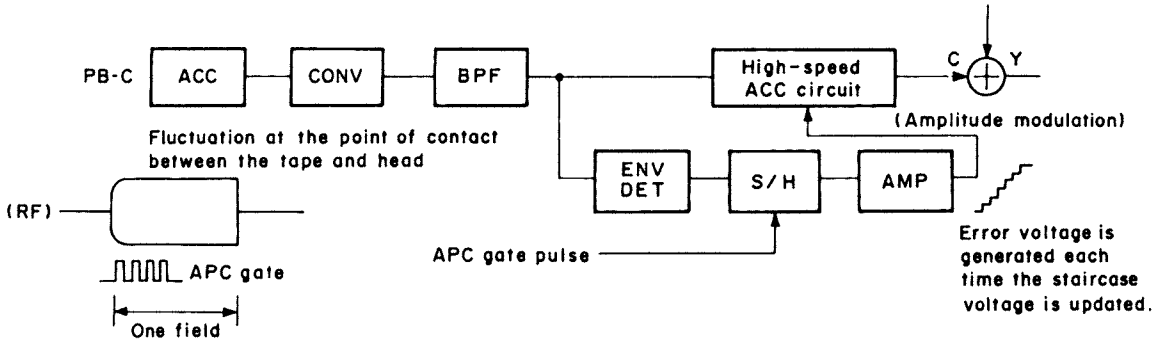


Fig.2-13. High Speed ACC Circuit

2-13. DM-54 BOARD (Chroma System)

2-13-1. Preamplifier

CH-A is input to pin 24 and CH-B to pin 23 of IC1. They are then input to the preamplifier inside the IC1. The EE-12V signal used to mute preamplifier inside the IC1 is input to pin 38AB of this board. This signal is inverted by Q12, then input to pin 1 of IC1. Also, RV1 is connected to pin 22 of IC1, so the voltage from the 6V regulator Q1 is controlled to perform preamplifier DC balance adjustment.
The CH-A and CH-B preamplifier outputs can be respectively monitored at TP1 and TP2. The RF switching pulse is input to pin 18 of IC1. CH-A and CH-B RF outputs can be respectively monitored at TP2 (pin 17) and TP1 (pin 16). Incidentally, RV5 is used for adjusting the channel balance of the RF chroma signal.

2-13-2. Audio Bias Trap

The playback chroma RF signal whose channel balance has been adjusted by RV4 is input to the low-pass filter FL501 via the buffer Q2, and the 688kHz chroma signal component is extracted. Q501 is an audio bias trap which traps the audio bias that leaks into the 688kHz chroma signal in the audio insert mode. LV501 is a bias leak adjustment to minimize the bias leak.

2-13-3. Chroma Amplifier

The EE chroma RF signal is input to pin 8B of CN103. DL501 is a delay line used to match Y and C delays. It equalizes EE chroma RF signal and EE Y-RF system phases, and sends the signal to pin 5 of IC502. The playback chroma RF signal is output from pin 1 of IC502, then input to pin 1 of the chroma amplifier IC503. The output signal is taken from pin 6 of IC503, then divided into two branches: the time-code detector and the delay circuit.

2-13-4. Time Code Detector

The playback chroma RF signal is input to pin 13 of the time code detector IC505 via RV503. RV503 is used for detection level adjustment of time code signal, and level can be monitored at TP502. The chroma signal whose level has been adjusted is input to the waveform shaper, then output from pin 1 (TP503) of IC505 via a 2-stage monostable multivibrator. A pulse that goes to "high" level is appears at TP503 where time code is inserted. An active "high" blanking pulse is input to pin 9 of IC505, so that the circuit only operates during the V-blanking period.

2-13-5. Delay Circuit

The playback chroma RF signal is input to pin 7 of IC503 via RV501. RV501 is used for playback chroma RF signal level adjustment. The signal whose level has been adjusted is input to the delay line DL502 via the low-pass filter FL502. DL502 is a 50nsec per step tap-select type delay line which sets Y/C delay for SP format system within ±25nsec. The signal delayed by DL502 is input to pin 3 of IC504 via the delay circuit Q550 in the SP mode, and to pin 5 of IC504 via the delay circuit Q505 in the conventional mode. RV524 and RV502 are used for delay time fine adjustment in the SP and conventional modes respectively. Incidentally, the output signal selected at IC504 can be monitored at TP501. Noise mixed with the chroma signal is muted by Q501 during the time code period. Pin 1 of IC504 output is input to the ACC amplifier at pin 5 of IC512. The chroma signal whose level became constant is fed from pin 3 (TP528) of IC512 to pin 1 of IC510, and it is amplitude-modulated. The RV516 inserted between pin 4 and pin 1 of IC510 is used to perform DC balance adjustment of the balanced modulator IC510.

2-13-6. DG Compensator

The Y signal is fed to RV513 via the buffer Q509, its level is adjusted and it is input to pin 8 of IC510. Q519 is a muting circuit for the DG compensator in the EE mode. The DG-compensated Y signal can be monitored at TP510. RV514 performs IC510 amplifier gain adjustment and ACC level adjustment. The DG-compensated chroma signal output from pin 6 of IC510 passes through the buffer Q520 and is divided into two branches: one goes to IC506 for DUB and the other is input to pin 2 of IC512 for the main line.

2-13-7. DUB Chroma Processing Circuit

The chroma signal input to pin 11 of IC506 for DUB is input to pin 7 of IC506 via DL504 and DL506. DL506 is a 50nsec/step delay line which performs Y/C delay adjustment of the DUB chroma signal. The level of the signal input to pin 7 of IC506 is adjusted by RV504, then the signal is output from pin 2 of IC506. The chroma signal is muted by the active "low" COLOR OUT signal input to pin 4 of IC506 when the played back signal is in B/W mode.

2-13-8. Main Line Chroma Processing Circuit

The 688kHz chroma signal can be monitored at TP515 and it is input to pin 2 of IC512. The 688kHz chroma signal is frequency converted to 3.58MHz and output from pin 24 of IC512. This output signal is input to the bandpass filter FL503, and the 3.58MHz component is extracted. The FL503 output is input to pin 13 of IC512, and the chroma signal is amplified. The amplified chroma signal is divided into two branches ; one is fed to the ACC detector and to the REF oscillator circuit inside the IC512, and the other is output from pin 11. The signal output from pin 11 can be monitored at TP518. This signal is divided into two branches : one is input to chroma buffer Q536, the other is integrated by R641 and C601, presence of the chroma signal is detected by Q533, inverted by Q534, and it is used for muting.

2-13-9. ACC Loop

The high speed ACC circuit detects the envelope of the playback chroma RF signal input to pin 11 of IC516. The burst flag pulse is input from pin 9 of IC515 to pin 7 of IC516. The playback chroma RF signal input to pin 11 of IC516 is sampled by the burst flag pulse, then envelope information is held. This held signal is input to pin 13 of IC516 and amplified, then fed to Q544. Q543 and Q544 are circuits used to mute the high speed ACC loop when a dropout compensation pulse is input during TBC operation and during V - blanking periods . Compensation level of the error signal output from TP530 is adjusted by RV521, then it is input to pin 2 of IC517, activating the high speed ACC circuit. RV522 is used for IC517 amplifier gain adjustment. The chroma signal output from pin 1 of IC517 is output via the Q545 buffer. It can be monitored at TP523.

2-13-10. APC Loop

The 3.58MHz chroma signal input to pin 13 of IC512 is input to the burst gate circuit inside the IC512. The burst gate pulse is input to pin 16 of IC512, the burst signal is extracted according to the timing of this pulse, and input to the APC detector. The APC detector compare the phase between the extracted burst signal and the 3.58MHz reference signal input to pin 15, and the detected phase error voltage is output from pin 14. This phase error voltage is input to pin 14 of IC511 to drive the VCO (Voltage-Controlled Oscillator) generating a frequency equal to 8 times 688kHz. The VCO center oscillation frequency is determined by the DC voltage apply to pin 19 of IC511. This voltage can be adjusted by RV505. The VCO outputs is divided by 8 by the internal down counter of IC511, becoming 688kHz. This 688kHz signal is frequency-converted by the internal reference oscillator (3.58MHz) to 4.27MHz, then output from pin 5. This 4.27MHz output is fed to the bandpass filter FL504, where its harmonics are removed, then it is output to TP513 via RV517. RV517 is used for 4.27MHz signal level adjustment. The 4.27MHz signal is input to pin 1 of IC512 to frequency-convert the 688kHz input signal into 3.58MHz. The DC voltage at pin 19 of IC511, which determines VCO center frequency, is controlled by IC507 in the TBC mode. This is because during TBC mode search tape-to-head relative speed changes, shifting the playback chroma carrier frequency. An APC ID (Identify) circuit has been included in the APC loop to prevent pseudo lock.

2-14. APC ID CIRCUIT

Pseudo lock occurs as follows. If, when power is turned on, the VCO ($\fallingdotseq 8\times688$kHz), which must oscillate at 350fH, for some reason starts oscillating at, say, 358fH, the 688kHz continuous wave becomes 688kHz+fH, the 4.27MHz carrier becomes 4.27MHz +fH, and the 3.58MHz chroma signal becomes 3.58MHz+fH. Since APC detection samples only the burst period at fH intervals, there is no APC error if the chroma signal is deviated by fH, so it is locked at 3.58MHz+fH. This is called pseudo lock. In this unit, condition of pseudo lock is detected by counting the frequency of the VCO by IC1. The actual counting method is as follows :

$$\begin{aligned} \text{VCO OUT} &\fallingdotseq 8\times688\text{kHz} \\ &= 8\times(44-1/4)\,\text{fH} \\ &= 8\times175/4\text{fH} \\ &= 350\text{fH} \end{aligned}$$

When counting the VIDEO OUT for a 4H period, the value

$350\times4\text{H}=1400$

is obtained, giving a 1/256 counter residual equal to

$1400-(256\times5)=120$

This value is compared with the upper (125) and lower (115) limits, and if it is outside this range an ID is output to return frequency to normal.

2-15. CHROMA NOISE CANCEL CIRCUIT

IC518 on the DM-54 board is the chroma noise cancel circuit which cancels a minute noise component generated by the amplifiers in the chroma signal.
A high frequency noise components are extracted by the HPF consisted of R692 and L522, and amplified by IC518. A positive and negative polarity chroma signals are obtained at pins 4 and 5 of the amplifier IC518 respectively, and they are diode-limited and mixed by RV523.
Since the output level at pins 4 and 5 of IC518 is different, the resulting mixed signal at RV523 becomes only a minute noise component.
The noise component is mixed (subtracted) with the main-line chroma signal to cancel the noise.

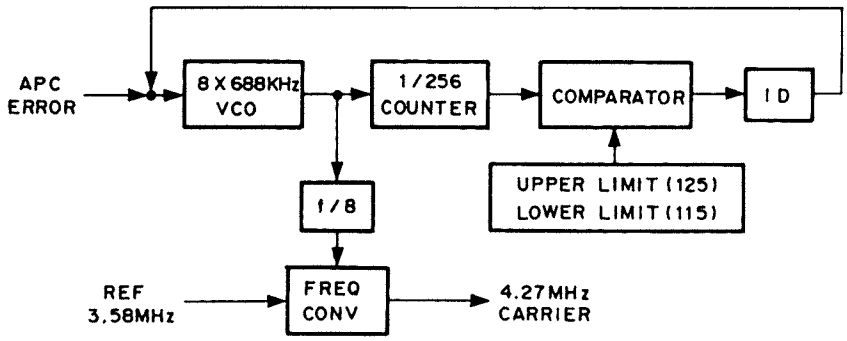


Fig.2-14. APC ID Circuit

SECTION 3
AUDIO SYSTEM

3-1. FEATURES

- Dolby C Type NR (Noise Reduction) Function
  Dolby C type NR system is employed in audio system together with the U-matic SP version. When Dolby is set to "ON", audio S/N ratio is improved over conventional machine. The high level/low impedance buffer amplifier is employed that improves S/N ratio when signal is transmitted among the circuit boards.

- Sendust Head
  Sendust head is installed that has been used in the BVU-850 already. It features small sized, stable high frequency characteristics and high durability against wear-out. Frequency response is 50Hz through 15kHz (±3dB). S/N ratio is better than 52dB (DOLBY NR OFF, RMS).

- Independent Audio Erase Circuit
  Separate audio erase circuits are prepared for audio CH-1 and CH-2, that are operating independently. By having two independent erase circuits, split edit (editing where video and audio are edited at different timings) becomes smooth.

- Relayless Circuit
  Relays that have been used for head switching and erase signal switching in BVU-800 and BVU-820 are no more used to improve reliability.

- Use of Exclusive Microcomputer for REC Timing Control
  In the previous U-matic VTR, there have been two problems in the audio insert editing, as listed below, due to mechanical distance between the erase head and the R/P head.
  ①Double recordings at IN point (recording twice)
  ②Non-recording area at OUT point
  Countermeasures for these problem are taken by means of hardware in the BVU-850. This equipment employs an exclusive microcomputer that controls erase and record timings by the software. The locked type oscillator is also employed at the same time so that these problems are solved and the editing accuracy is improved too.

3-2. REC/EE System

Since audio CH-1 and CH-2 have same circuit configuration, the audio CH-1 is mainly described as follows. Fig.3-1 shows REC/EE system block diagram. Fig.3-2 shows level diagram.

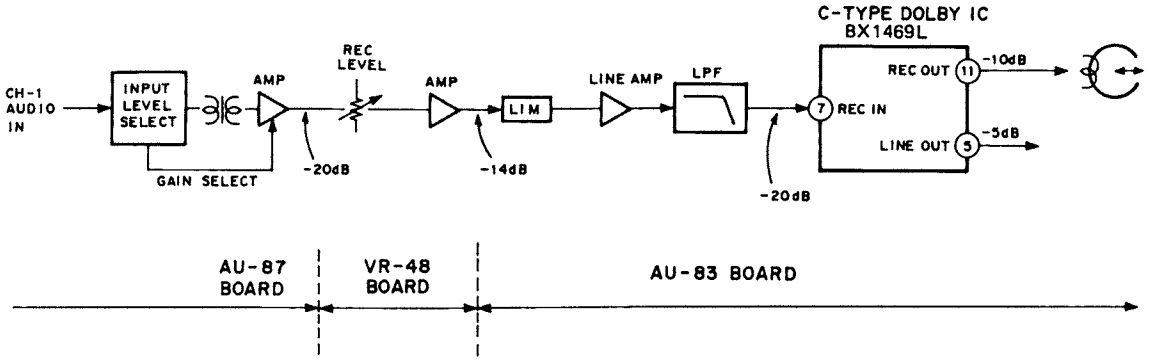


Fig.3-1. REC/EE System Block Diagram

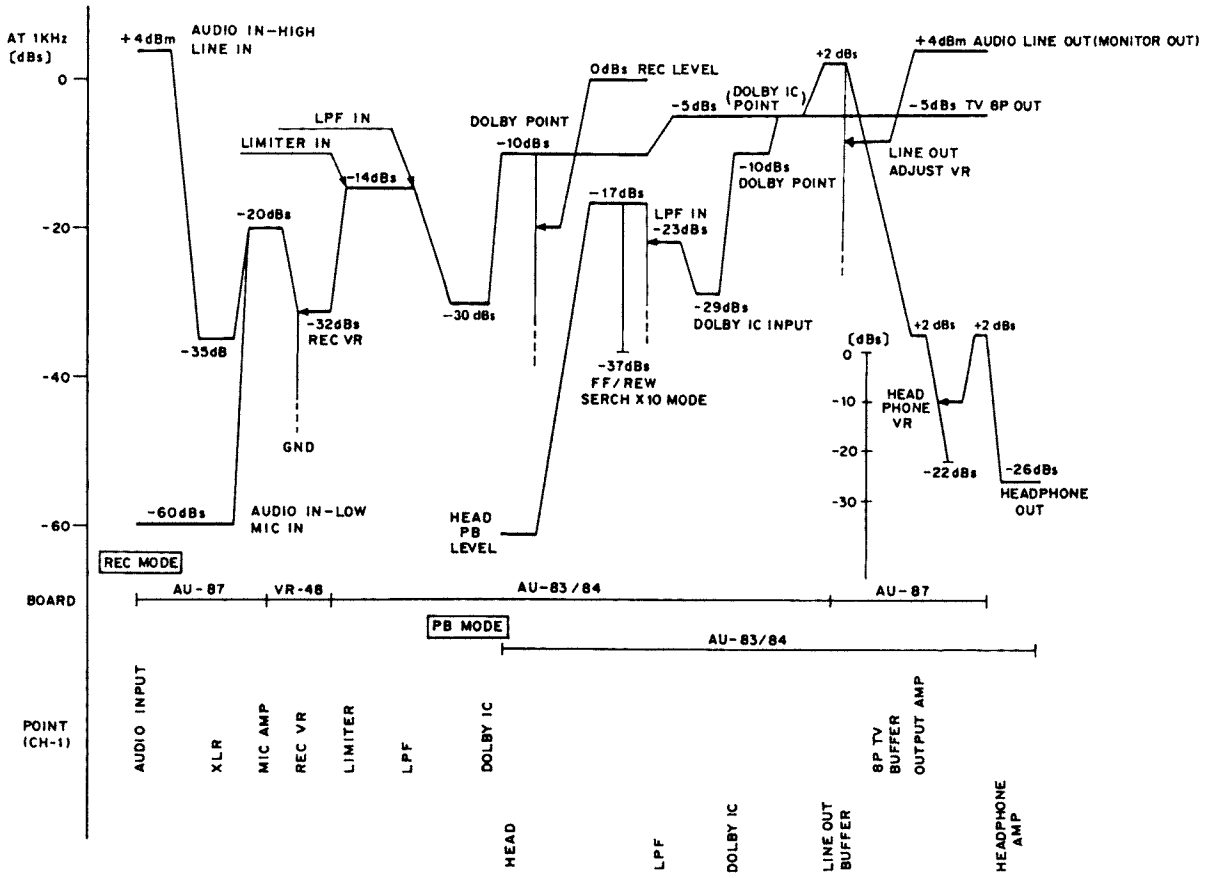


Fig.3-2. Level Diagram

3-2-1. AU-87 Board

Audio signal that is input to the AUDIO IN connector on the connector panel is input to pin 1 of CN871 on the AU-87 board, and then to input level select circuit. This circuit consists of 600 Ω termination switch and input amplifier. Input level selection is done by three position switch. The MIC IN (−60dBm) position selects "Low" and LINE IN (+4dBm) position selects "High" (600 Ω OFF) or "High" (600 Ω ON). By selecting SL1 through SL3 on the AU-87 board, input level in the LINE IN mode can be set to either one of +8dBm, +4dBm or −10dBm.
Input signal with +4dBm is attenuated to −35dBs by the attenuator consisting of R3, R6 and R7. S/N ratio is not much affected by this attenuation. The attenuated signal is then amplified to −20dBs by input amplifier IC1. This amplifier works as 40dB gain amplifier in MIC IN mode, and works as 15dB gain amplifier in LINE IN mode. Output level remains constantly −20dBs regardless of "Low" level input mode or "High" level input mode. Since input level to IC1 is different depending on input level select switch position, gain of the amplifier is controlled to that the output level remains constant by SW1 (4/4) selection. Input circuit is improved for better S/N so that Dolby effect can be exerted to full.

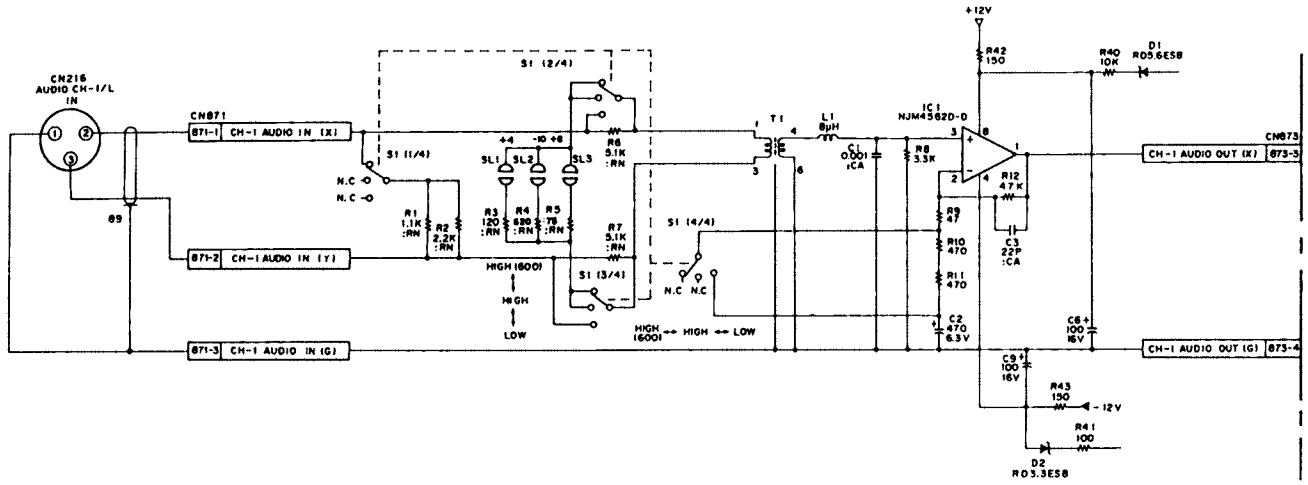


Fig.3-3. Audio Input Circuit

3-2-2. VR-48 Board

Output signal from the AU-87 board is input to this board. Signal's recording level is adjusted by RV3, amplified to −14dBs by IC1 (1/2), and is sent to AU-83 board.

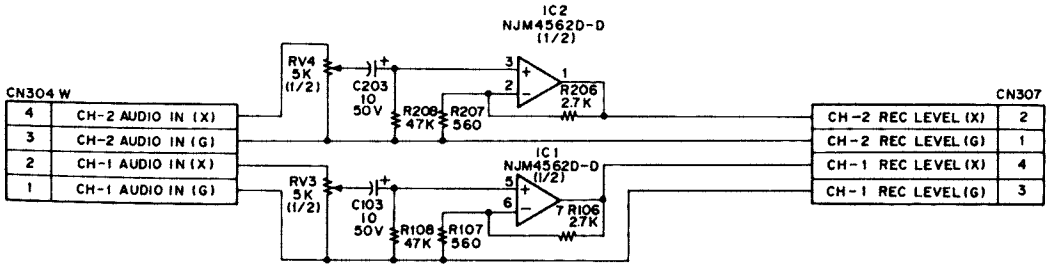


Fig.3-4. REC Amplifier

3-2-3. AU-83 Board

1. Limiter

This board receives −14dB audio recording signal from the VR-48 board via pin 3 of CN4, and sent to limiter consisting of Q15 through Q18 for amplitude limiting. This limiter operates only in record mode. In playback mode, "Low" level of the "LIMITER ON IN" signal is supplied from the BC-11 board that turn Q17 and Q15 on, so that limiter operation stops. When limiter is operating, the monitor amplifier IC6 (1/2) output is supplied to the base of Q18 via limiter level adjustment RV7, that is integrated by C34 and is input to the base of Q15 via Q16.

Q15 is controlled by the output level of IC6 (1/2) so that line output level at TP8 should be 2dBs by varying the input impedance of IC11 (1/2) and by controlling amount of attenuation. The recording signal is attenuated to −34dBs by limiter and attenuator. This signal is amplified by line amplifier IC11 (1/2) to +1dBs. The amplified signal is sent to low-pass filter CP2 having cut-off frequency of about 27kHz, and is supplied to attenuator consisting of R73 through R75, to be attenuated down to −30dBs. This signal is supplied to the subsequent Dolby system IC (IC3) pin 7 as its reference input level.

2. Record Amplifier and Equalizer

In order to process audio signal in the Dolby system, the record level and playback level should be of equal level. If record level and playback level are different, Dolby effect will not be fully exerted and also fluctuation of frequency response will be the result. This unit is designed that the TP4 level is −10dBs both in the record mode and the playback mode.

The record signal output from pin 11 of IC3 at −5dBs is routed to the high-pass filter IC4 that removes signal lower than 40kHz in order to prevent erroneous detection of pilot tone (it will be discussed later). The record signal is then sent to the record amplifier IC5 (1/2) where record signal is amplified and receives record equalization. Since SP tape and conventional tape have different high frequency response characteristics, either Q21 or Q22 is switched so that proper record equalizer characteristics and record level are selected. The record level can be adjusted by RV9. The level-adjusted signal is inverted and amplified by the next stage amplifier IC5 (2/2) and is sent to the bias trap circuit.

3. Bias Trap Circuit

Bias trap circuit consists of LV1 and C2. The bias-trapped record signal is mixed with 71kHz bias oscillator output that is supplied from the AU-85 board, and is recorded on tape via audio head in ac bias system. The record signal (TP7) before bias trapping is sent to the audio CH-2 circuit on the AU-84 board for cross-talk cancel.

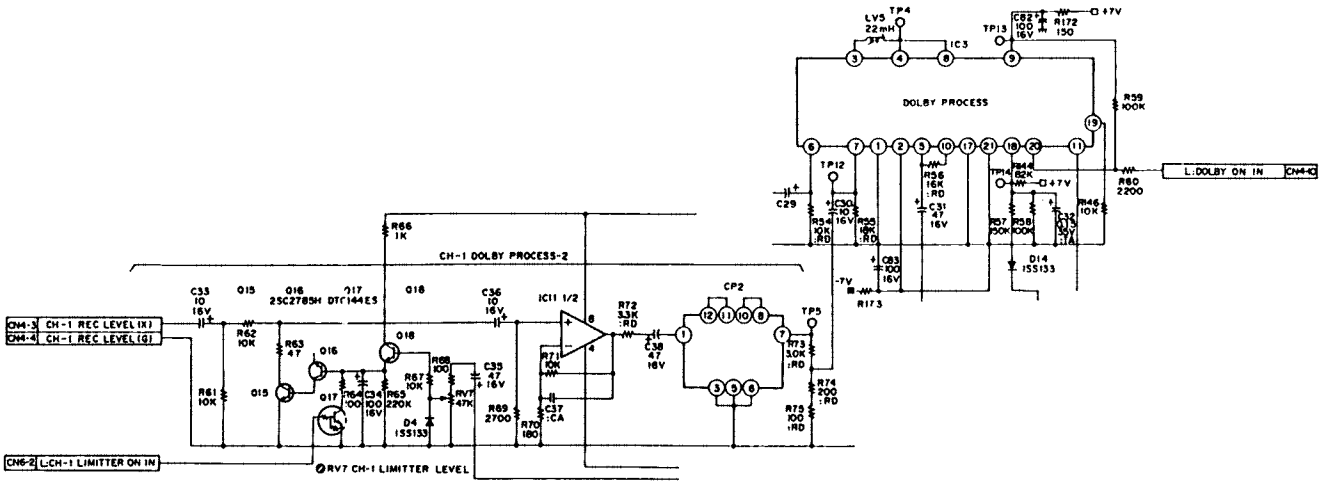


Fig.3-5. Dolby System Processor

4. Cross-talk Cancel Circuit

This circuit works only in audio insert mode. When audio CH-1 is put in record mode while audio CH-2 is put in playback mode, the audio CH-1 record signal at TP7 is supplied to the AU-84 board. This signal is supplied to the inverting input (−) terminal of CH-2 head amplifier IC1 (1/2) via RV1, RV2 and LV2 so that audio CH-1 cross-talk leaking into audio CH-2 playback signal is reduced. The EE mode LINE OUT signal is output from pin 5 of Dolby IC (IC3), and is amplified by line amplifier IC6 (1/2) to +2dBs via IC7. The amplified signal is divided into three outputs : output to the AU-87 board, output to the HEADPHONE connector through buffer IC6 (2/2) and output to CH-1 audio meter via Q31. The signal that is supplied to the AU-87 board is amplified by IC100 (1/2) to +4dBm and output from the LINE OUT connector via T101.

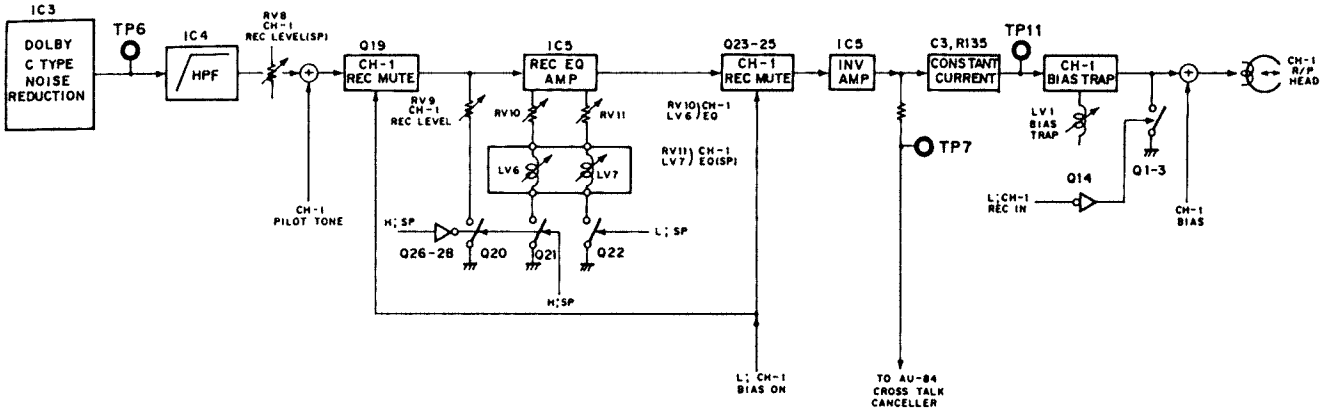


Fig.3-6. Cross-talk Cancel Circuit

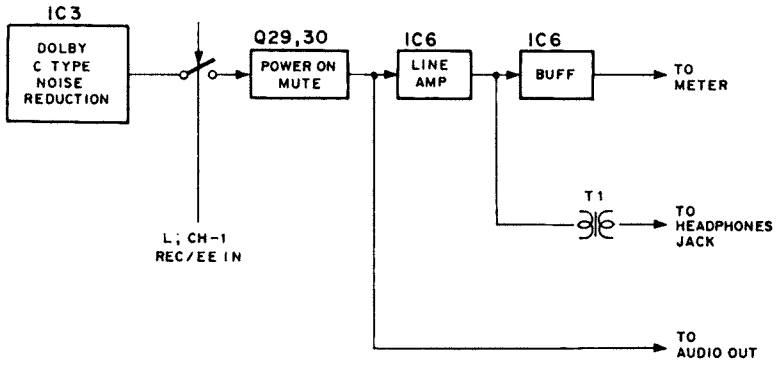


Fig.3-7. Audio Output Signals

3-3. PB System

The −62dBs playback signal that is reproduced from audio head, is input to pin 1 of CN3 on the AU-83 board. The input signal is passed through bias trap circuit consisting of C10 and LV3, and is amplified to −17dBs by head equalizer amplifier IC1 (1/2).

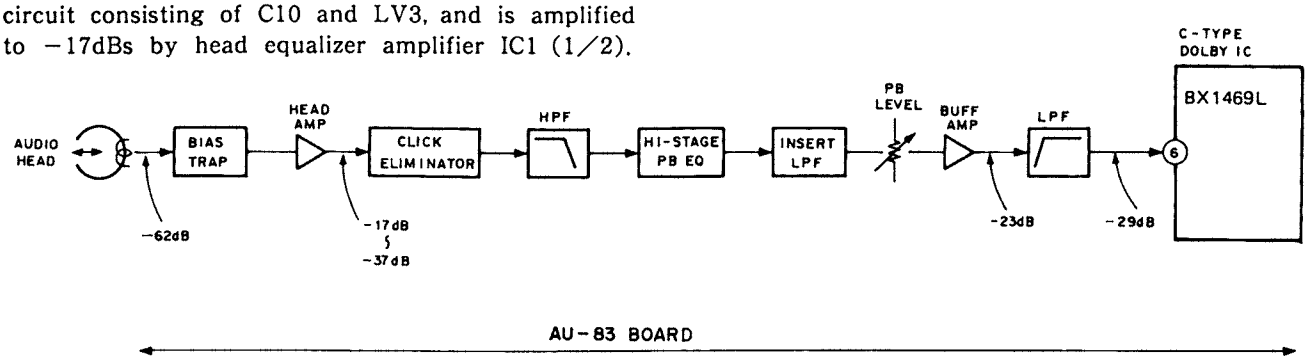


Fig.3-8. Playback System

3-3-1. Click Noise Eliminator

Since head equalizer amplifier IC1 (1/2) has higher gain of about 80dB in low frequency range, a noise bigger than signal level will be produced in the instance when unit is switched from record mode to playback mode or vice versa. In order to prevent click noise, Q6 is turned "on" so that low frequency signal change will not be amplified in the instance of mode change-over.

3-3-2. Pilot Tone Eliminator

A high-pass filter consisting of IC1 (2/2) and IC2, eliminates low frequency signal lower than about 40Hz in order to remove 15Hz pilot tone. The 15Hz component is suppressed lower than −50dB.

3-3-3. Cross-talk Canceler

Q10 is turned "on" when either one channel is put into insert mode so that high frequency signal around 20kHz is suppressed and cross-talk is reduced. Playback signal receives frequency response adjustment by RV4, RV5 and LV4. The signal level is adjusted by RV6. The playback signal is passed through low-pass filter CP1 having cut-off frequency of about 27kHz, attenuated to −29dBs by attenuator consisting of R51, R52 and R53. The signal is then input to Dolby circuit (IC3 pin 6). The output line signal from Dolby circuit (IC3 pin 5) at −5dBs is input to the VR-48 board via pin 3 of CN5. The input signal receives level adjustment by RV3 on the front panel and is again input to the AU-83 board. This signal is input to the line amplifier IC6 (1/2) via the analog switch IC8. The line amplifier is muted by Q29 and Q30 in the instance when power switch is turned on for the period of C60 charging time. The line amplifier output is sent to the AU-87 board via pin 9 of CN5, feeding LINE OUT connector at the range from −∞ to +6dB with reference level of +4dBm.

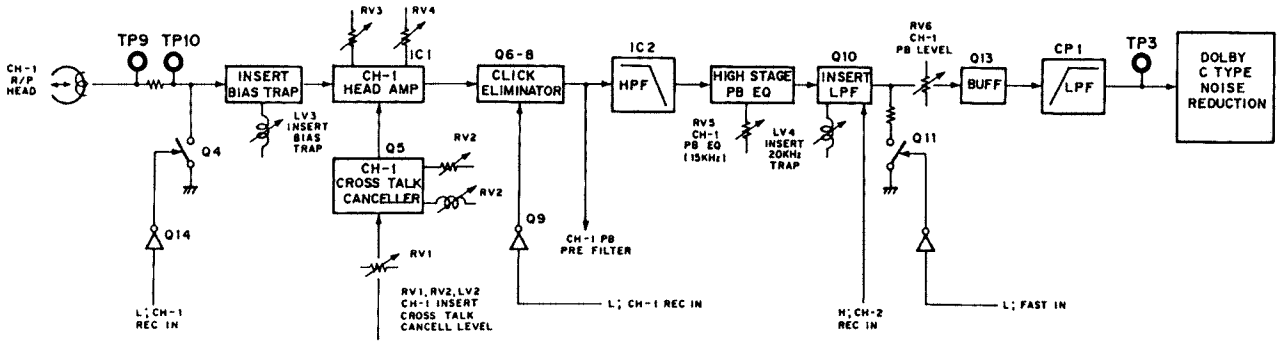


Fig.3-9. Dolby System

3-4. Bias/Erase Oscillator (BC-11 Board)

Crystal oscillator X301 output is divided by 32 by IC302 to produce 71kHz that is supplied to the AU-85 board. Microcomputer controls video and audio recording timings. This exclusive microcomputer functions in preventing sound-missing or double recording.(See system control description).

"High" level of "OSC ON" signal is output from pin 48 of microcomputer IC401 that set the 71kHz oscillator circuit consisting of IC301, IC302 and X301 to enable condition. The 71kHz clock signal is supplied to four blocks of the AU-85 board (CH-1 erase driver, CH-2 erase driver, CH-1 bias driver and CH-2 bias driver). Since the frequency of CH-1 and CH-2 bias drivers are locked to 71kHz, beat interference due to bias frequency does not take place. IC101 and IC102 are bias current amplifier that selects bias current automatically depending on SP tape and conventional tape for their optimum recording level. When SP tape is used, "Low" level of "SP IN" signal is input to B22 terminal of the AU-85 board that turns Q127 off so that specified bias current determined by RV3 and RV5 is supplied to the head. When conventional tape is used, bias current is adjusted by RV4 and RV6 for respective channels. Therefore, bias current adjustment should start with SP tape by RV3 and RV5, and then proceed to K tape current adjustment by RV4 and RV6. SP tape bias current is higher than conventional tape bias current by about 20%.

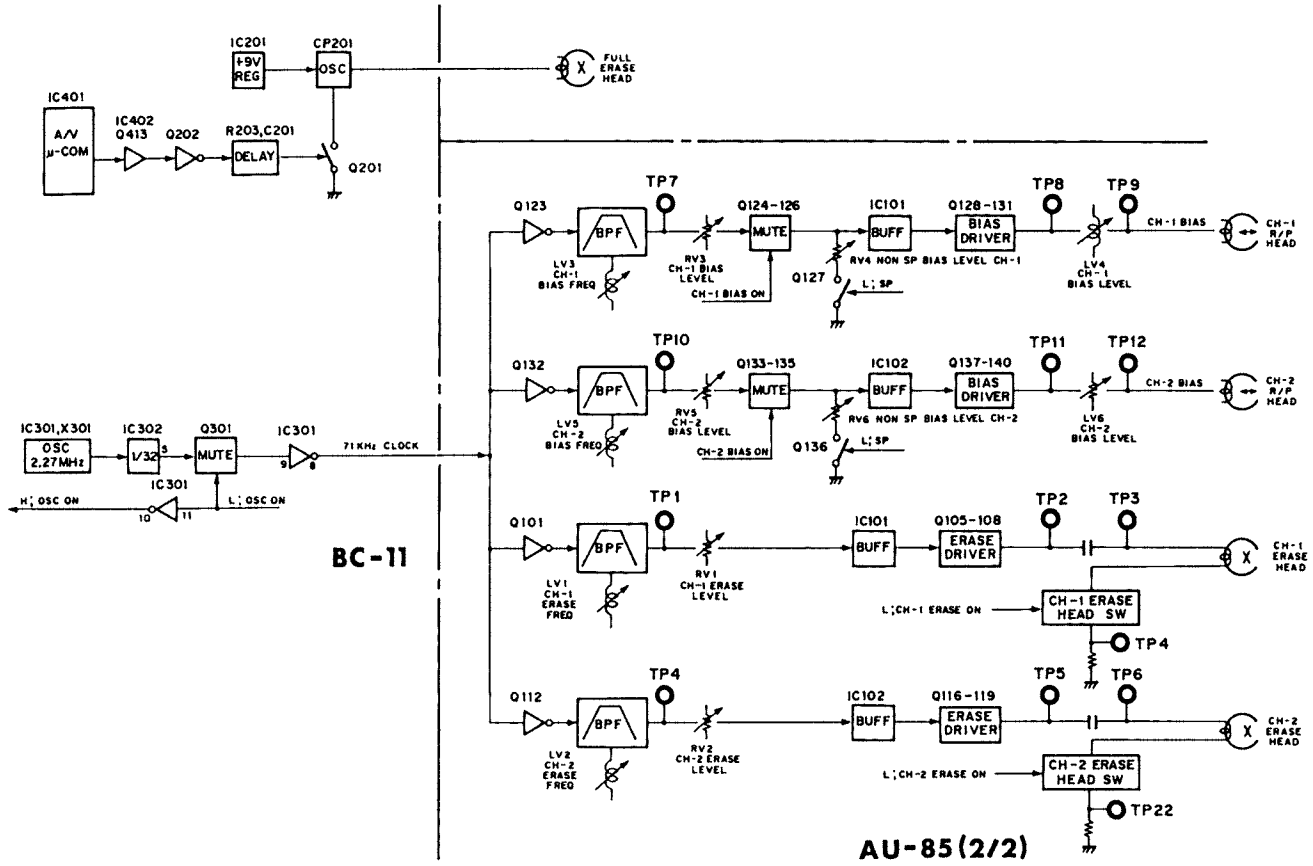


Fig.3-10. Bias/Erase Oscillator

3-5. Dolby Mode Detector (AU-85 Board)

Dolby recording is possible for SP tape only in this unit. Dolby recording is not possible in K tape. The Dolby switch can specify whether recording is made in Dolby mode or non-Dolby, by its ON/OFF position. When recording is made with the Dolby switch set to ON, 1/4 VD (15Hz) signal is mixed with audio signal as pilot signal and recorded on tape. Dolby ON/OFF is automatically set regardless of Dolby switch position in playback mode by detecting the 15Hz of pilot signal component.

3-5-1. Pilot Signal Recording Circuit

During Dolby recording mode, the 1/2 VD signal selected by the servo system is input to terminal B31 of this board as CTL signal. The 1/2 VD signal is divided into two so that 30Hz is divided into 15Hz by D type flip-flop IC1. The 15Hz is converted into sinusoidal wave by low-pass filter IC2. The pilot signal is thus produced and is phase-shifted by phase shifter IC2 until it has same phase with that of recording CTL signal. The pilot signal is then output from terminal B24 via level adjustment circuit consisting of Q10 through Q13. The pilot signal is mixed with audio signal in the AU-83 board and AU-84 board and is then recorded on tape.

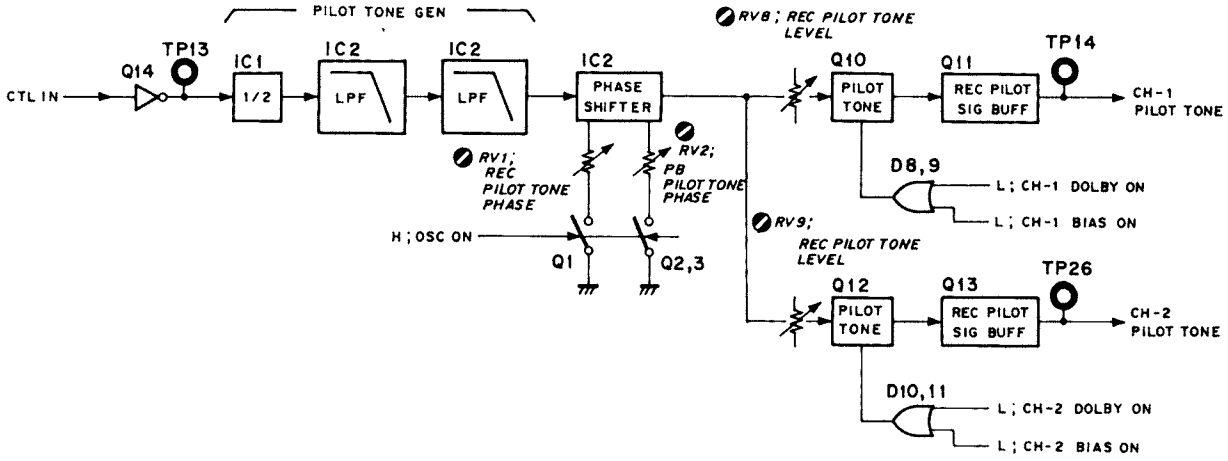


Fig.3-11. Pilot Tone Detector

3-5-2. Pilot Tone Detector (PB)

This circuit detects 15Hz pilot tone signal that is recorded with audio signal in Dolby mode. The output signal of playback amplifier IC1 (1/2) is supplied to low-pass filter IC3 where low frequency component (15Hz) is extracted and is input to phase detector IC4, IC5 and IC502. The 1/2 CTL signal is at the same time input to IC1 whose output phase is adjusted by IC2 and RV2 and input to phase detector IC4. The 1/2 CTL signal that is phase-inverted by Q146, is input to IC5. The pilot tone is detected by phase detector IC4 and IC5 where 15Hz component in the playback audio signal is multiplied by 15Hz that is generated by dividing the playback CTL signal. It is to say that, if 15Hz signal component is in phase with 1/2 CTL signal, it detects that the pilot tone is incoming. If the pilot tone signal and 1/2 CTL signal are 180 degrees out of phase, "High" level signal is output from either D1 or D2. RV4 is the dc balance adjustment for Dolby detector output, that is adjusted for equal dc level at TP17 and TP18.

3-5-3. Dolby Control Circuit

In the BVU-850, Dolby detecting logic circuit is installed in audio board, however, all the Dolby system in this unit is controlled by microcomputer that is installed in the BC-11 board. The Dolby mode detector output signal is supplied from the AU-85 board to CN14A on the BC-11 board, and the signal is processed by microcomputer IC401 by software means.

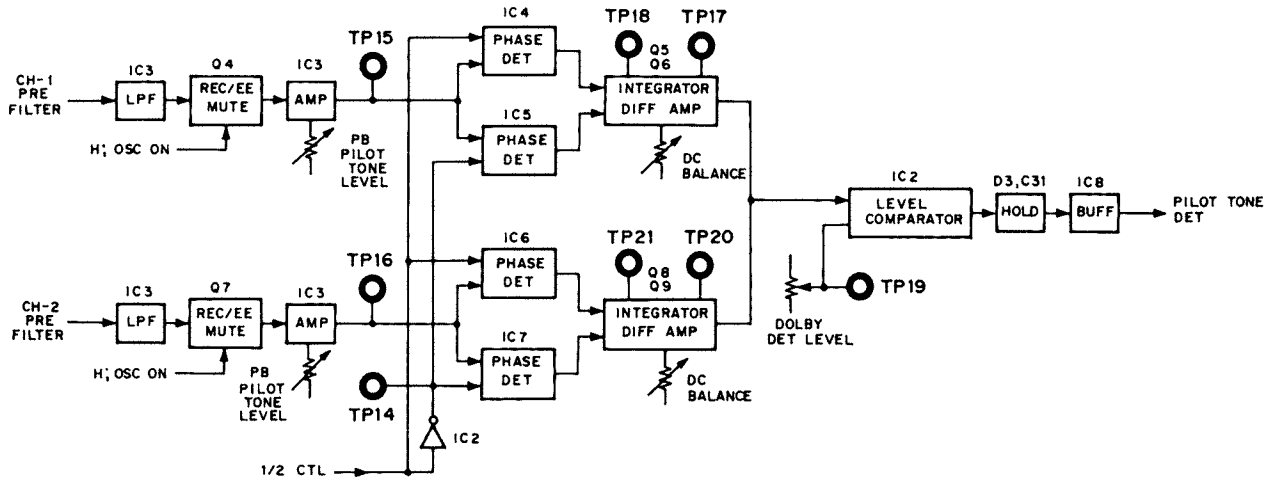


Fig.3-12. Pilot Tone Detector (PB)

SECTION 4
SERVO SYSTEM

4-1. OUTLINE

In the conventional BVU-800 series, the drum, capstan and reel servo circuits were composed of four printed circuit boards, and the drum and capstan servo systems have been configured with the CX194 digital servo IC.
In consideration of simplification of the printed circuit board, the BVU-950 uses a single microcomputer and its peripheral circuit, and control the drum, capstan and reel servo systems.
The μ PD78310 8-bit (16-bit inside) single-chip microcomputer, newly developed and manufactured by Nippon Electric Company (NEC) is employed as the servo microcomputer.

4-2. MICROCOMPUTER PERIPHERAL CIRCUIT

IC407 on .the SV-88 board is a 16/8-bit microcomputer for the servo system. It contains a RAM, A/D converter, CTC and I/O controller. It controls the servo circuit while communicating with the microcomputer M2 (IC7) located on the SY-102 circuit board.
The peripheral circuits of the microcomputer consist of four 16-bit timer counter (CTC) ICs three 16-bit interval measuring ICs (ITMR), three I/O expanders serving for the input/output port expansion of the microcomputer, a ROM and RAMs.
The sync signal, drum PG, capstan FG, reel FG, tension detector, CTL signal and other informations entering the SV-88 board are processed by discrete circuits and the microcomputer's software, and the microcomputer controls the servo through D/A converters.

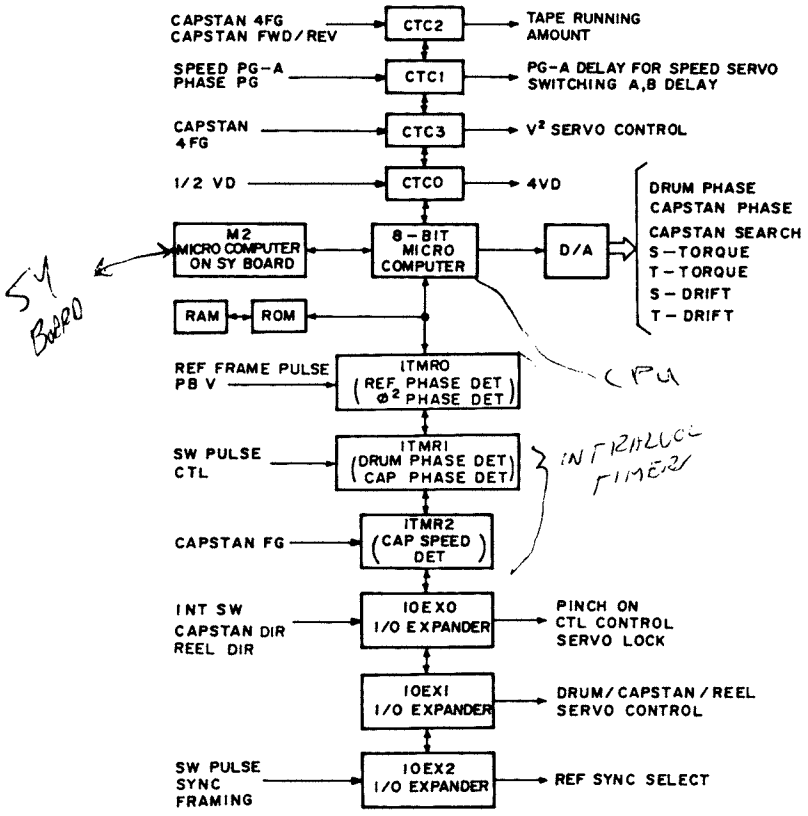


Fig.4-1. Microcomputer Peripheral Circuit

4-3. MICROCOMPUTER

The microcomputer μPD78310CW is provided with an 8-bit data bus and 16-bit address bus. Bits 0 through 7 of the address bus and the 8 bits of the data bus are employed as common bus, and the information is processed on a time-sharing basis. The latch IC406 is provided to share the bus. When the H : ALE signal from pin 55 of the microcomputer IC407 is output, the microcompurter processes the bus as an address data. The data bus and address bus are connected to the IC404 2K RAM and IC405 128K ROM, and the data bus is further connected to the CTCs and I/O expander.

IC408, 409 and 410 are the address decoders of the abovementioned ROM, RAM, CTCs and I/O expander. Pins AN0 through 3 of the microcomputer IC407 are the analog input pins of this microcomputer, and their input data are A/D converted inside the microcomputer and processed digitally. These 4 analog inputs are sent from the multiplexers IC402 and 403 which serves as the microcomputer analog input port expansion. The circuit consisting of Q405, 406 and D403 through 410 is limiting the analog input voltage approximately 0V to +5V.

Pins 21 through 24 of the microcomputer are the port for communicating with the microcomputer M2 on the system control board, and IC413 is the buffer of this port. A system clock for the microcomputer is the 12MHz clock signal generated by IC420 and X401. The divider IC422 provides the 6MHz, 1.5MHz, 188kHz and 47kHz clock frequencies from this clock signal. These frequencies are used for the CTC clock, phase detection clock and capstan/reel 4FG detection clock signals.

The P04 to P17 output port of the microcomputer is a digital output port for the servo data which have been processed inside the microcomputer. The digital output is converted into an analog value by the D/A converter IC411. A current output is obtained at pins 18 and 19 of IC411, and this is converted into a voltage by IC412. The voltage level for the D/A conversion is adjusted by RV402.

The outputs of D/A converter are sent to 7 system, including the drum phase system, capstan phase system, capstan search system and reel torque system, processed by the sample and hold circuits consisting of IC414 through IC417 and C420 though C427.

The D/A converted output is adjusted by RV402 so that the DC voltage at TP402 operates centering on 2.5V. A 0V voltage is produced when all 12 bits of the D/A converter are "0" and a 5V voltage is obtained when they are all "1". IC418 and IC401 are the reference voltage generator.

The 5V and 2.5V reference voltages are obtained at TP403 and TP404, respectively. The 5V reference voltage is used as the reference voltage for A/D conversion inside the microcomputer and as the reference voltage of the D/A converter IC411.

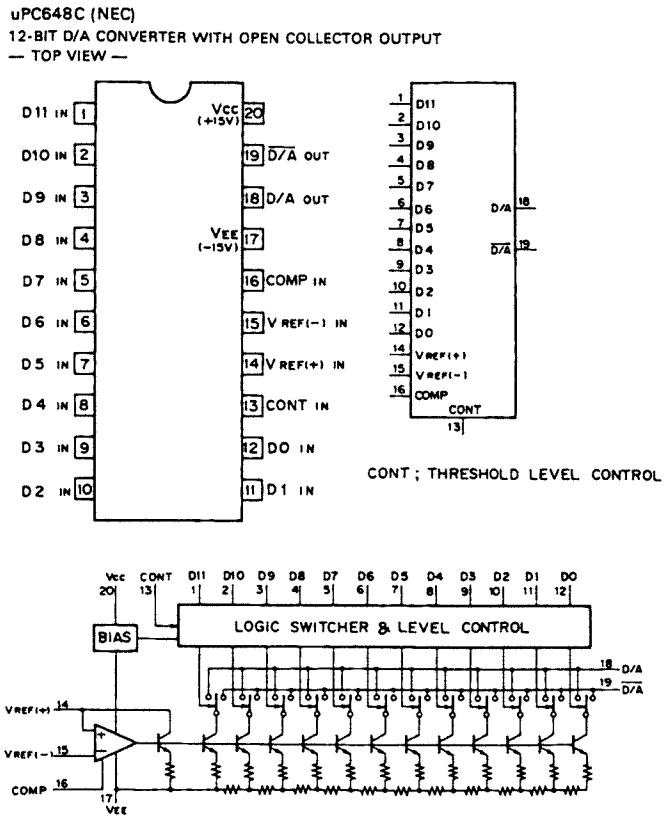
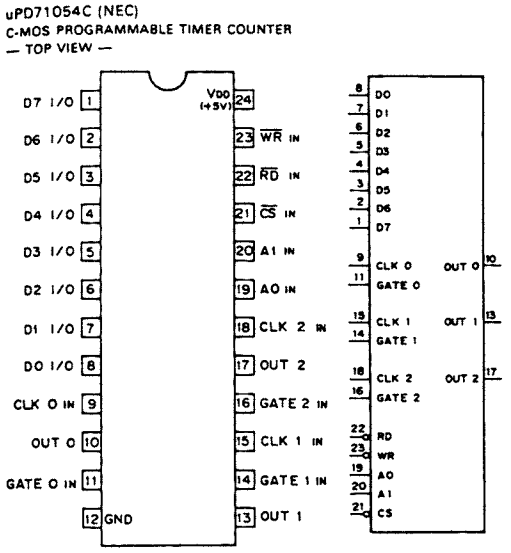


Fig.4-2. D/A Converter

4-4. CTC (IC301 to IC304)

The μPD71054C is a CMOS type of programmable timer/counter and 3-channel timer/counter is provided inside this single chip. The 3-channel counter/timer starts counting the clock inputs while the respective gate pins are set high in accordance with the CTC program. The count results are output from the OUT pins and read into the microcomputer. The counter/timer program is determined by the control word given in the following function table.



FUNCTION TABLE

INPUTS					FUNCTION
CS	RD	WR	A1	A0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Control Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No-Operation (Hi-Z)
1	X	X	X	X	Disable (Hi-Z)
0	1	1	X	X	No-Operation (Hi-Z)

D7-D0 ; 8-BIT DATA I/O
CLK 0-2 ; COUNTER CLOCK
GATE 0-2 ; COUNTER GATE
OUT 0-2 ; COUNTER OUTPUT
RD ; READ COUNTER
WR ; WRITE CMD OR DATA
CS ; CHIP SELECT
A0,A1 ; COUNTER SELECT

0;LOW LEVEL
1;HIGH LEVEL
X;DON'T CARE
HI-Z;HIGH IMPEDANCE

Fig.4-3. CTC

4-5. SERVO AND SYSTEM CONTROL COMMUNICATION

The command and status communications between the servo system and system control is performed by the serial communication. This communications line is in common with AV microcomputer.

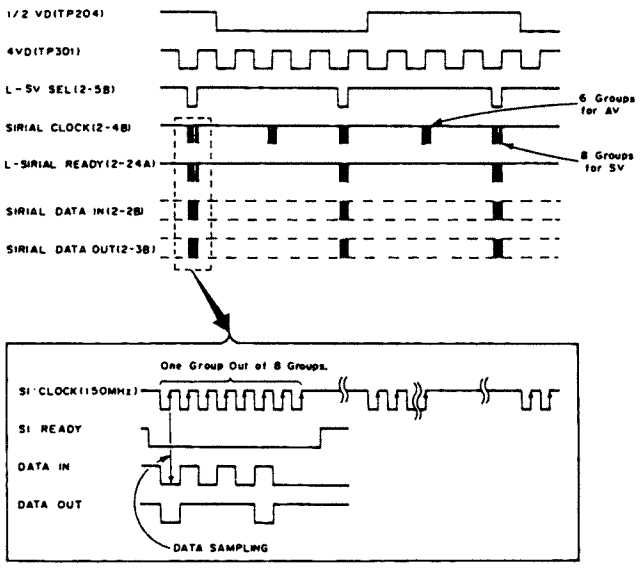


Fig.4-4. Waveformes For The Communications

4-6. REFERENCE SYNC SELECTOR

The reference sync selector is located on the SV-88 board. Provided for the reference sync signals are 3 signals : the reference video input signal from the rear panel, the black burst signal from the plug-in TBC board and the input video signal from the MD board.

The reference video input signal from the rear panel and the black burst signal from the TBC board are input respectively into pins 3 and 5 of the switcher IC101 on the SV-88 board. These two signals are switched by the signal from pin 60 of IC120 (I/O expander). In other words, the TBC black burst signal is selected when the plug-in TBC is being used, and the reference video signal is selected when the playback signal is locked to the external TBC or locked to the reference video input. The sync signal is separated from the selected signal by IC102 and is input to the switcher IC105. IC104 detects the reference sync signal and it advises the microcomputer via the I/O expander as to whether this signal is present or not.

The switcher IC105 serves to establish either the signal selected by the above-mentioned switcher or the sync signal of the input video signal, as the reference sync signal. This switching differs according to the position of the REF SYNC selector switch on the rear panel and the mode of VTR.

IC106 through 109, IC115 and IC117 configure the frame pulse generator circuit, pulses are output frame by frame at TP103 as a servo reference.

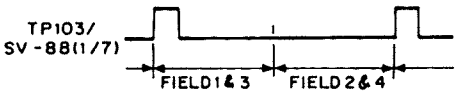


Fig.4-5. Frame Pulse

4-7. PB V PULSE DETECTOR

The sync signal that is separated from the PB video signal, is input from the DM board to pin 17A of CN2 on the SV-88 board. This signal is inverted by Q102 and the V sync signal is separated by IC111, IC112 and IC125, the resulting signal then passes through TP105 and is supplied to the ϕ^2 servo circuit as the PB V pulse. The IC113 detects whether the playback V sync signal is present or not by the pin 12 input signal, and it outputs a high signal to pin 9 of IC113 when the V sync pulse does not arrive within the R163 and C130 time constant.

4-8. SWITCHING PULSE GENERATOR

The switching pulse generator is composed of IC114 and IC116 through IC118. The waveforms of the drum speed PG-A and phase PG signals are shaped on the SV-88 board, and the signals are respectively input into pins 2 and 1 of the binary counter IC114. The phase PG pulse and the timing pulse produced by shifting the phase of the phase PG pulse by 180° are output by the counter IC114 and the pulses are respectively input into the two monostable multivibrators (IC116). The two timing edges are delayed in the monostable multivibrators (IC116) to adjust the switching position. The signals output from pins 7 and 9 of IC116, first pass through the digital delays based on the CTC, they enter the AND-gate IC117 and then input to pin 11 of IC118 where they are latched. The output of pin 13 of IC118 enters pin 5 of the next IC118 and is locked to the playback H SYNC signal. The switcher IC105 outputs the H-locked switching pulses when the playback sync signal exists and it outputs the latch output when the sync signal does not exist.

The pin 11 of AND-gate IC117 output is input to the two monostable multivibrators (IC119) to generate the vertical blanking pulse and the pseudo VD signal. The pseudo VD signal is the pulse which is inserted into the video output in order to stabilize the vertical sync in the search mode.

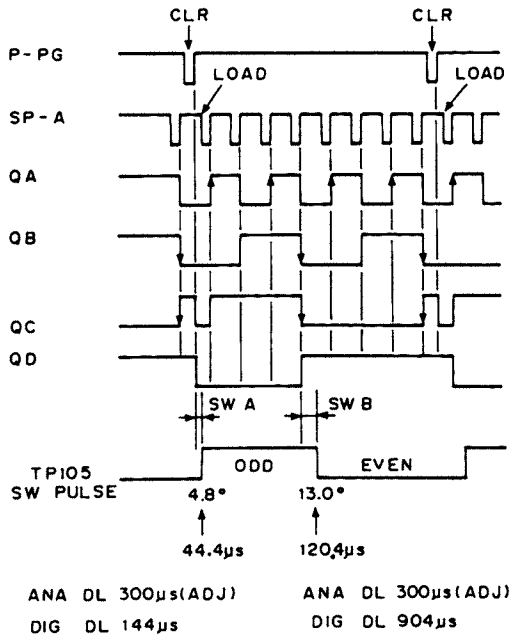


Fig.4-6. Switching Pulse Generator

4-9. ROTARY ERASE MUTING PULSE GENERATOR

This circuit generates the muting pulse so that the time code track signal will not be erased by the rotary erase current during video insert editing. The waveforms are shown in the figure below.

The drum speed PG-A pulse is input to the monostable multivibrator IC113, and after the RE HEAD timing whose phase is advanced for 32° from the original switching pulse, has been adjusted, it enters the shift register IC122. Referenced to the phase PG signal, the "H/L" timing pulse which is equivalent to 4PG is provided by IC122, and the CH-A and CH-B mute pulses are generated by the two monostable multivibrators (IC123). The timing equivalent to 4PG signal corresponds to half a drum cycle.

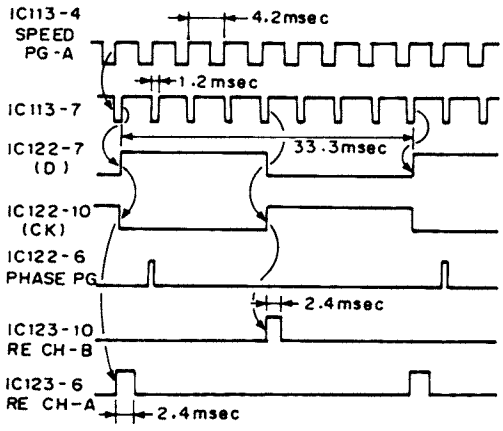


Fig.4-7. RE Muting Pulse Generator

4-10. DRUM SERVO

Fig.4-8 is a rough block diagram of the drum servo system. As in the conventional servo system, there are three drum servo loops: the speed system, phase system and AFC (search mode) system loops. Only the speed system loop is configured by hardware which, more specifically, is based on an analog circuit. Both the phase system and AFC system are controlled by the software by using the microcomputer.

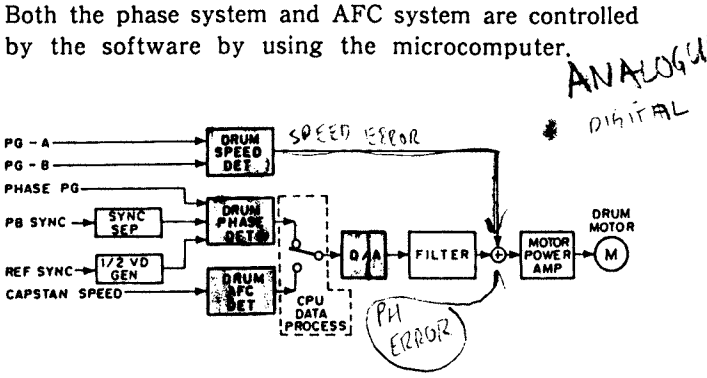


Fig.4-8. Drum Servo

IC514 is the ramp generator which is charged by the C545 and R804 time constant and reset by Q508. Meanwhile, the PG B pulse is waveform-shaped by IC511, and a sampling pulse is created by IC513. The drum speed is detected by the sample and hold circuit composed of Q509, C546 and IC514, and it is mixed by the next IC515.

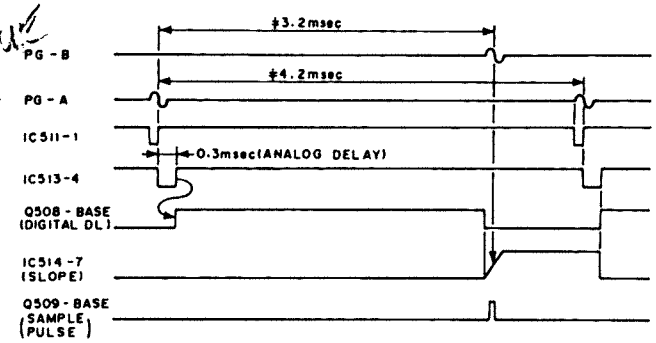


Fig.4-9. Drum Speed Servo

4-10-1. Drum Speed Servo

The configuration of the drum PG is the same as that used in the type 7 and type 9 systems, it is characterized by the PG (A) and PG (B) speed PG coils for the speed PG magnets for generating 8 pulses with every turn of the drum, and by the phase PG which generates one pulse for every turn. The drum speed servo measures the time difference between speed PG (A) and PG (B). The ramp waveforms generated from PG-A signals are sampled with PG-B signal and the sampled signals are compared to the reference voltage to produce the speed detection voltage.

The drum speed loop system is located on the SV-88 board. Fig.4-9 shows the waveform of the drum speed system. The drum speed PG A pulse is input to pin 21B of CN1 on the SV-88 board where its waveform is shaped by IC511. The PG A signal is then divided into two. One signal is delayed by the speed monostable multivibrator for speed detection and the other signal is sent to the switching pulse generator. For speed error detection, the PG A signal is delayed by the monostable multivibrator IC513. RV506 adjusts the free speed of the drum. The pin 4 of IC513 output is supplied to the gate of CTC1 at pin 11 of IC302 on the SV-88 board where it is delayed digitally. The digitally delayed signal is output from pin 10 of CTC1, inverted by IC307 and supplied to the base of Q508 on the SV-88 board.

4-10-2. Drum Phase Servo System

The drum phase servo system functions to maintain a stable phase relationship between the 1/2 VD signal provided from the reference sync signal and the pulses generated by the phase PG signal. It is also provided with the ϕ^2 servo which matches the playback V sync phase with the reference V sync phase in order to stabilize the phase servo during editing.

The drum phase error is detected by comparing the reference 1/2 VD signal phase and SW pulse (delayed phase PG) phase. The phase is compared by channel A of the IC309 (ITMR1). The switching pulse generated by the drum phase PG is supplied to pin 14 of IC309 and the 1/2 VD signal synchronized with the reference sync signal is supplied to pin 13. The difference between the phases of the two signals is measured by using the 1.5MHz clock signal which is supplied to pin 17. This information is supplied to the microcomputer through the data bus, processed inside the microcomputer, and the phase error is output as the D/A output.

4-10-3. ϕ^2 Servo System

The ϕ^2 servo system is an additional phase servo to the normal drum phase servo in order to safeguard against servo fluctuations at the edit points.
The ϕ^2 servo system functions so that the phases of the playback V sync and reference V sync signals during playback are matched in the editing mode. This phase relationship is maintained during insert editting.
The phase of two signals is compared by channel B of IC308 (ITMR0) on the SV-88 board. The reference V sync and playback V sync pulses are supplied respectively to pins 15 and 16 of IC308, and the phase difference is detected inside IC308. The error information relating to the phase difference is sent through the data bus to the microcomputer, and the microcomputer's software serves to control the drum servo through compensating for the drum phase error by means of ϕ^2 ERROR signal.

4-10-4. Drum AFC Servo System

In the search mode when the TBC is not being used, the relative speed of the video heads and tape will vary which means that the horizontal period will change and the H sync of a monitor will not lock. To prevent this, the drum AFC servo system controls the rotations of the drum so that the relative speed is made constant.
The conventional CX194 featured an AFC servo system which employed the playback H sync signal for control so that the horizontal period was kept constant. However, the AFC speed may be changed by the guard band, and so the BVU-950 uses a capstan FG signal to control the drum speed in accordance with the tape speed.
The capstan 4FG signal is employed to detect the capstan speed. The capstan 4FG signal and capstan direction signal are input respectively to pins 9 and 14 of IC301 (CTC0). Those informations are supplied through the data bus to the microcomputer, and voltages corresponding to the speed and direction of the capstan are output by the microcomputer through the D/A converter.
The drum phase error voltage and AFC error voltage are supplied to pin 6 of IC515 on the SV-88 board where they are amplified. RV507 serves to adjust the operating voltage during the drum phase lock mode and AFC mode. The switcher IC607 selects wheather the drum phase error integrator is ON or OFF during recording.

4-10-5. Picture Splitting Compensator

"Picture splitting" is a jitter occurring every one rotation of the drum which is caused by eccentricity in the drum or by the fluctuations generated by drum cogging. If the picture splitting components are too large, the monitor screen will appear to be broken up by vertical lines.
Two monostable multivibrators (IC512) are used to compensate these components and cancel them by mixing them with the drum speed loop. These two monostable multivibrators generate the desired phase and amplitude voltage from the 30Hz switching pulses, and the errors are applied to the drum motor. The phase is adjusted by RV504 and the amplitude by RV505.

4-10-6. Drum Motor Driver

The drum speed error and phase error are input to pins 3 and 2 of IC515 where they are mixed and then sent to the motor driver on the DR-53 board. D512 supplies the voltage for starting the drum motor. The drum current is detected by R6 on the DR-53 board, and it is fed back to the mixing amplifier IC515 through pin 20B of CN2 on the SV-88 board to compensate the drum motor cogging.

4-11. CAPSTAN SERVO

Fig.4-10 is a simple block diagram of the capstan servo.
There are six loops in the capstan servo system. Except for the capstan speed servo system, all the servo systems are controlled by the microcomputer. These loop systems will now be described briefly.

1. Capstan Normal Speed System

This system is a loop for controlling the speed of the capstan motor which is also employed for the servo using the conventional CX194. In the BVU-950, it is configured by an analog circuit in the same way as with the drum speed system.

2. Capstan Normal Phase System

This loop system is the same as that which is employed for the servo using the conventional CX194, although this loop system operates only during normal playback. As with the conventional control method, control is exercised so that the phases of the reference 1/2 VD and playback CTL signals are matched.

3. Instant Start System

This loop system functions only while normal playback has started and it is a loop for speeding up the capstan start-up. When the tape speed is adjusted from prerolling during editing, this system serves to speed up the capstan phase synchronization and quickly lock the capstan servo.

4. REC Speed System (V^2 Servo)

This is a servo loop system which was not provided with the conventional U-matic VTRs. It functions only during the recording mode.
The conventional capstan phase servo system during recording was characterized by the comparison of the reference 1/2 VD signal and capstan FG signal which was counted down. In the V^2 system, however, the motor is controlled in the recording mode by exercising another loop of speed control besides the speed servo in 1. This means that if the capstan motor rotates at a constant speed during recording, this loop will exercise control so that the frequency of the capstan FG will be made constant by the microcomputer.

5. Search Speed Loop System

In the search mode, the normal speed and phase loops are isolated and the capstan motor is controlled by applying the voltage corresponding to the search speed commands.
The voltage, which corresponds to the capstan search commands with speeds ranging from −5 times to +5 times normal tape speed, is output and the motor speed is controlled.

6. Stop/Brake Control Loop System

This system controls the capstan motor so that the guard band noise, generated in the still picture mode, is positioned at either the top or bottom of the monitor screen.
The stop servo is also applied to prevent the tape from being moved by the shock of external disturbances or noise from the position where it has stopped. The capstan brake control system serves to detect sudden deceleration commands such as FWD 5 times to STILL or REV to FWD, and to brake the capstan.

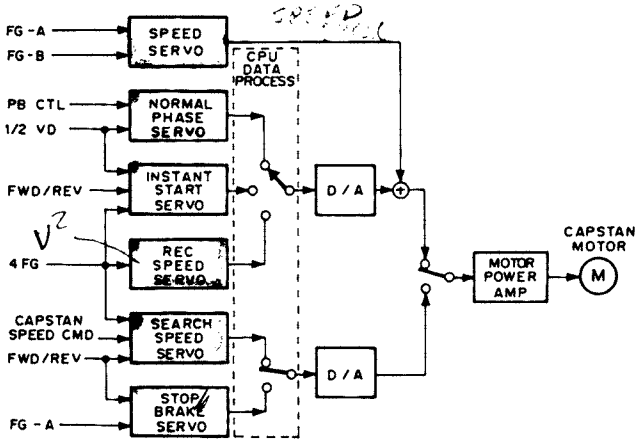


Fig.4-10. Capstan Servo

4-11-1. Capstan Speed Servo

The capstan speed servo system is composed of analog circuitry on the SV-88 board.
This servo controls the capstan speed by detecting the time difference between the FG A and FG B signals sent from the DMEs (divided magneto-resistive elements) mounted on the capstan assembly. The frequency of the capstan FG in the conventional U-matic VTRs was 450Hz but this has been made 454.23Hz at 1 time speed in the BVU-950. The FG A and B signals from the DME elements are first amplified by the FG amplifier in the capstan assembly to approximately 1Vp-p and they are then supplied to the SV-88 board. These signals are shaped into rectangular waveforms by the two operational amplifiers (IC501). The input circuit of IC501 is characterized by band-pass filter characteristics for improving the wow and flutter.
The FG A signal is input to the base of Q502 and a ramp waveform is provided by IC502. The capstan free speed is adjusted by RV501. The FG B signal is input to the monostable multivibrator IC509 and a sample pulse of the ramp waveform is output. The speed detection voltage, which has been sampled and held by Q503 and C509, is sent to the mixing amplifier IC503 via the buffer IC502 and IC504.

4-11-2. Capstan Phase Servo

The capstan phase servo is a servo loop system which functions only during normal playback. It controls the capstan motor so that the phases of the 1/2 VD signal and playback CTL signal are mached.
In this servo system, the phase error is detected in channel B of IC309 (ITMRI) on the SV-88 board. The information of the phase error detected in IC309 is read into the microcomputer via the data bus and processed. The phase error is output from the P04 to P17 port of the microcomputer and D/A converted by IC411. It is then sampled and held by IC144, C420 through C427, IC416 and IC417, and it passes through the switcher IC505 on the SV-88 board.
Although pins 5 and 4 of switcher IC505 are normally connected, in the instant start mode the pin 3 side is connected, the amplifier gain of the next stage is increased by R501 and phase synchronization is accelerated. In the capstan phase servo, the phase relationship between the playback CTL signal and the 1/2 VD signal is aligned by the tracking potentiometer. The tracking potentiometer information is read into the microcomputer through pin 14 of IC402 on the SV-88 board, it is converted into digital data inside the microcomputer and processed.

4-11-3. Capstan Motor Drive Circuit

The capstan error voltage mixed at pin 2 of IC503 is supplied to the amplifier IC504. The capstan motor employed in this unit should be applied only a positive voltage to control the motor speed, and it uses the direction commands of different pins to control in the reverse direction. This is why IC504 is an amplifier which outputs only a positive voltage. Depending on the relationship between the detected voltage and the reference speed voltage of the capstan, the pin 1 of IC503 output a positive or negative voltage. When it is a negative voltage, Q505 is turned ON and so IC504 functions as an inverting amplifier.
The pin 1 of IC504 output enters the switcher IC505 which serves to switch between the normal loop system and search loop system. The error voltage is then sent to the DR-53 board through the buffer IC504 and then to the capstan motor through the motor driver.
Switcher Q507 on the SV-88 board is for turning the capstan motor on and off. The capstan motor is started by applying the search voltage when the motor should be started.

4-11-4. Instant Start Servo

Under normal playback conditions, the phase error is detected in the capstan phase servo system by comparing the phases of the playback CTL and reference 1/2 VD signals. Phase comparison is carried out every 30Hz cycle. In contrast, the instant start servo compare the phase using capstan 4FG, which speeds up the phase loop synchronization. This makes it possible as a result to provide smooth synchronization during editing.
Provided in the software of the microcomputer are the VD counter which is reset by the 1/2 VD signal and the FG counter which is reset by the CTL signal. These two counters are compared at the 4VD period, the difference between the two counter values (phase difference) is output from the microcomputer and passed through the D/A converter to control the capstan motor.
The figure below illustrates in diagramatic form the software inside the microcomputer when the tape speed is 3/4 times normal speed.

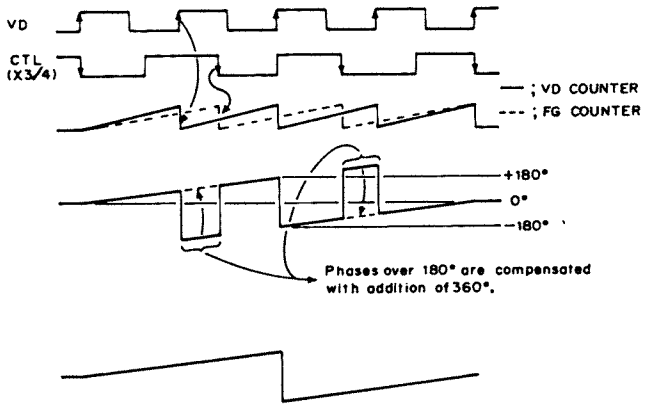


Fig.4-11. Instant Start Servo

4-11-5. REC Speed Servo (V² Servo)

With the conventional capstan phase servo employing CX194 during recording, the frequency of the FG under normal speed conditions had to be 450Hz so that the frequency could be divided by either 18 or 15. This was because of the relationship with the frequency division ratio (15 for NTSC and 18 for PAL). This meant that the relationship between the diameter of the capstan shaft and the number of teeth in the frequency generator had to be kept in a constant relationship.

The V² servo measures the accurate clock pulses during a capstan period and compensates the speed servo system so that this time agrees with the rating. The adoption of the V² servo obviates the need for this relationship between the diameter of the capstan shaft and the number of capstan FG teeth.
A block diagram of the V² servo loop is shown below.

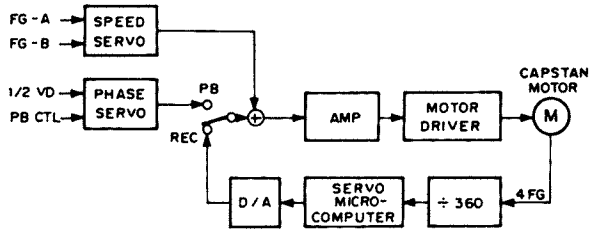


Fig.4-12. V² Servo Loop

There are 90 teeth in the capstan FG, the 4FG frequency is divided down by 360 and the pulses generated for each turn of the capstan are supplied to the microcomputer. The microcomputer counts up the number of 0.19MHz clock pulses during a single period of the capstan, it compares this with the reference count and outputs the difference.
The period equivalent to a single turn of the capstan is measured by IC303 (CTC3) on the SV-88 board. The V² start signal is input to pin 10 of IC305 and when this is set to low, pin 9 of IC305 is set to high, the signal is latched by the 4FG signal supplied to pin 3, and the count is started by supplying the signal to pin 11 and 14 of gate input of the IC303 (CTC3). The pin 11 of IC303 input detects a single turn of the capstan, and so when it is divided down to 1/360 by CTC, a low level signal is output from pin 10, the flipflop IC305 is reset and the count is concluded. The 0.19MHz clock pulse used for counting is supplied to pin 15 of IC303 and the period of the capstan turn is measured by channel 1 of CTC3. The results of the measurement are passed through the D/A converter and then through the same loop as the capstan phase system, and the speed system is compensated for.

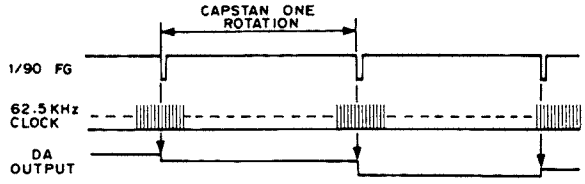


Fig.4-13. Capstan FG Count Timing Chart

4-11-6. Search Speed Control

A search control circuit is provided in order to stabilize the tape speed in the capstan drive search mode (1/30 to 5 times normal tape speed in both forward and reverse directions). The capstan speed in the search mode is determined by the search command information sent from the system control. The capstan FG signal is supplied to pins 13 and 14 of IC310 (ITMR2) on the SV-88 board in order to detect the capstan speed information. Based on this capstan speed information, the search speed error is converted into a DC voltage by the D/A converter IC411, it is passed through the sample & hold circuit composed of IC414, C422 and IC416, and it is supplied to pin 12 of IC504 on the SV-88 board. The error voltage which is amplified by IC504 is switched to the normal loop by the switcher IC505 and the motor speed is controlled.
In a low-speed search mode, the capstan FG signal for detecting the speed is switched to the 4FG signal, and the precision of the speed is increased. The capstan 4FG signal is supplied to pins 15 and 16 of IC310 on the SV-88 board.

4-11-7. Capstan Stop Servo

The capstan stop servo functions to prevent the tape from moving in the still picture mode. The FG signals, generated by the rotation of the capstan, are used for this. There are 90 teeth in the FG ring of the capstan motor. If this is made equivalent to a frame (30Hz), then the frequency generator corresponds to 15 teeth. In the stop servo, this is further doubled and 30 stop locations are set.
When the machine is in the still mode in the phase such as in Fig.4-14, a voltage is applied in the reverse direction to the motor by means of the tape tension difference, provided that a forward direction force is exerted, and the tape will stop at the stop position. This processing is conducted by the microcomputer, and the detected error signal drives the capstan motor in the same loop as that for the search speed.

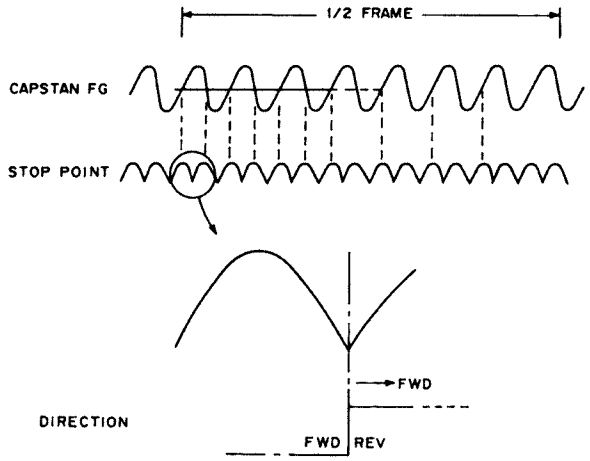


Fig.4-14. Capstan Stop Servo

4-11-8. Capstan Brake Control

The capstan motor must have a brake to deal with sudden changes in the tape speed. The timing for applying the brake is produced by the microcomputer detecting the capstan speed using FG signals, which is read into the microcomputer through IC310 (ITMR2) of the SV-88 board, and the brake voltage is applied through the search loop system.

4-12. REEL SERVO SYSTEM

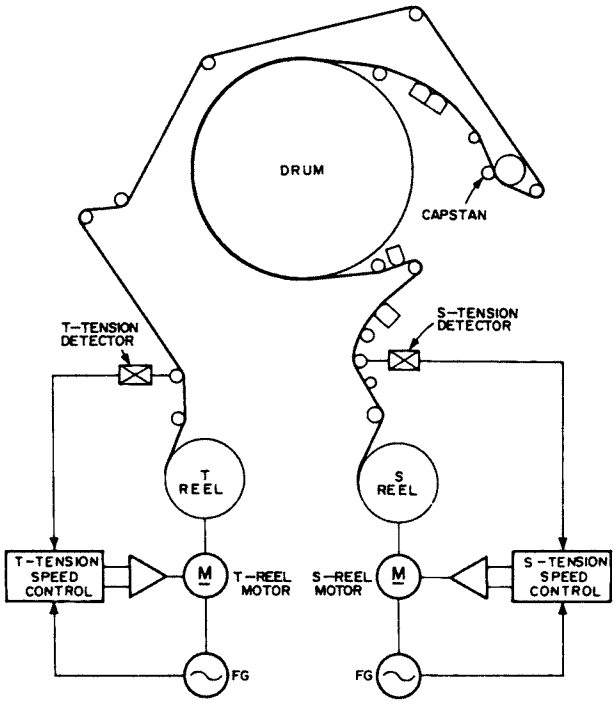


Fig.4-15. Electrical Reel Servo

4-12-1. Electrical Servo

The magnetic tape is loaded from the supply reel table and is rewound onto the take-up reel table. This machine features a direct-drive dedicated DC motor both for the supply and take-up reel tables.
The rotation of the two reel tables is controlled by the current which are applied to the DC motors. In other words, the rotations of the reel tables are controlled by the electrical reel servo system.
When the DC motor speeds up or slows down, the rotation of the reel table increases or decreases accordingly.
Magnet rings with 48 magnets are provided at the side of the take-up and supply reel tables. The change in the magnetic field is detected using the DME elements. The DME output is 96 cycles per rotation. The rotational speed of the reel tables is detected using the DME outputs.

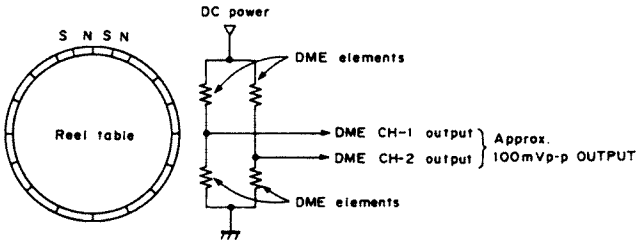


Fig.4-16. Reel Table Rotation Detector

- Magnet rings with 48 magnets are provided on the reel table, and output is 96 cycles per rotation
- DME elements are located close to the reel table and mounted on the SE-48 board.
  CH-1 and CH-2 outputs are phase-shifted by 90 degrees.

Note : DME is abbreviation for Divider type Magneto-resistive Element.

4-12-2. Tape Tension Detector

When increasing or decreasing the reel motor torque, the tension applied to the tape (tape tension) will be increased or decreased accordingly.

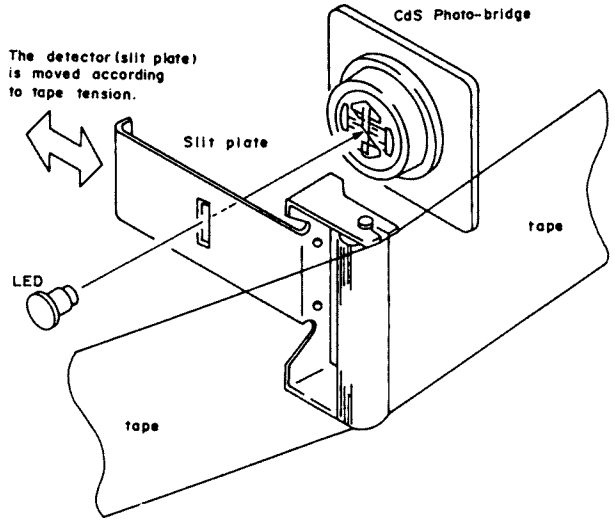


Fig.4-17. Tape and Tape Tension Detector

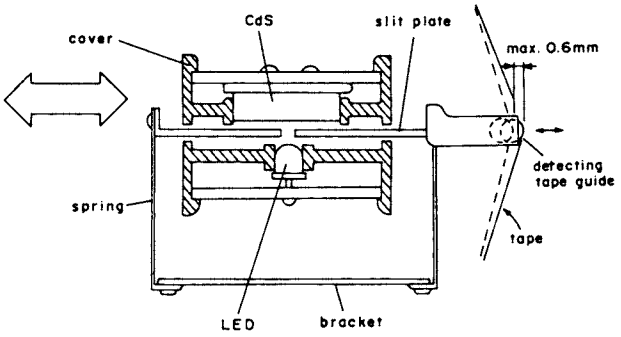


Fig.4-18. Tape Tension Detector

Two tape tension detectors are provided in the tape transport path and they detect the tape tension at both the supply and take-up sides separately. The tension detectors are composed of a combination of LED and CdS photo-bridge. Light from the LED passes to the CdS photo-bridge. Between the LED and CdS photo-bridge is a slit plate serving to cut off the light which is supported by a plate spring. When the tape tension increases, this slit plate is pushed in.

When the position where the light from the LED applies changes, the voltage output from the CdS photo-bridge changes (drops). This makes it possible to ascertain the tape tension at any time.

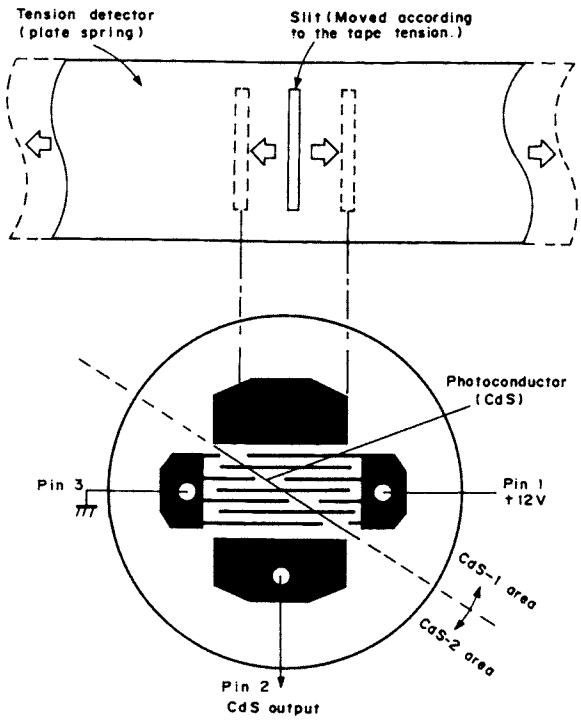


Fig.4-19. CdS Photo-bridge Pattern

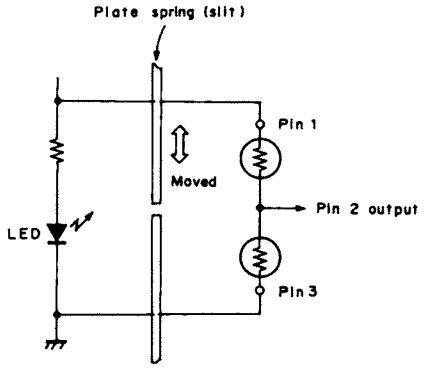


Fig.4-20. Construction of Tape Tension Detector

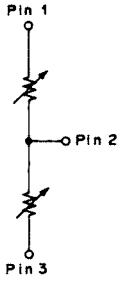


Fig.4-21. Equivalent Circuit of CdS Photo-bridge

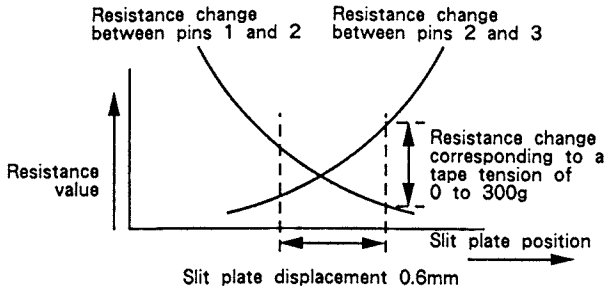

Resistance change between pins 1 and 2
Resistance change between pins 2 and 3
Resistance value
Resistance change corresponding to a tape tension of 0 to 300g
Slit plate position
Slit plate displacement 0.6mm

Fig.4-22. Relation Between Tape tension and CdS Output

4-13. CONFIGURATION OF REEL SERVO

A part from the acceleration compensation by using the capstan motor current and AC feedback areas, all operations in the block diagram are processed by the microcomputer.

The reel servo system is provided on the SV-88 board. Two reel motors are controlled in each mode by detecting the tape tension and rotational speed for T and S sides.

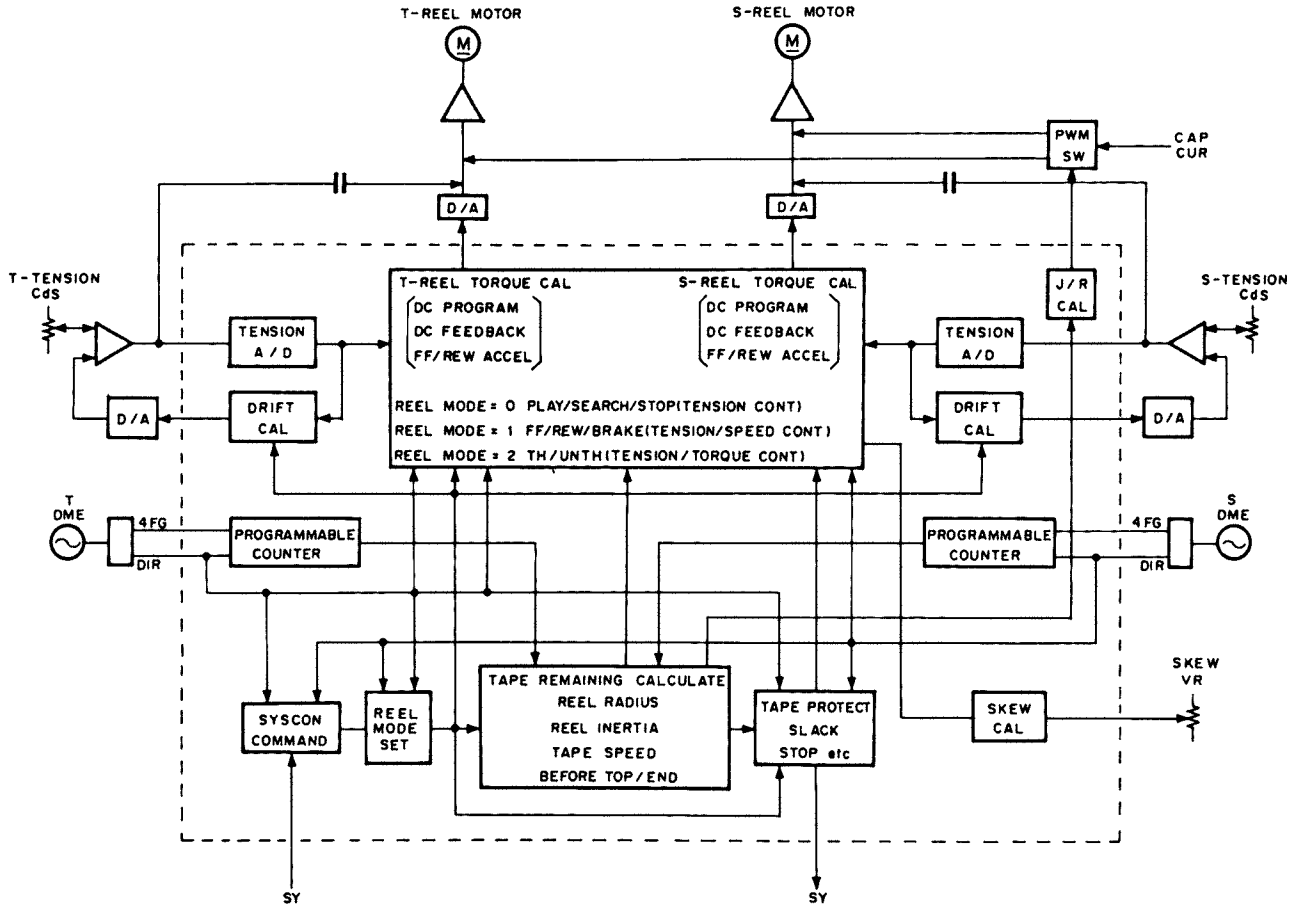


Fig.4-23. Configuration of Reel Servo

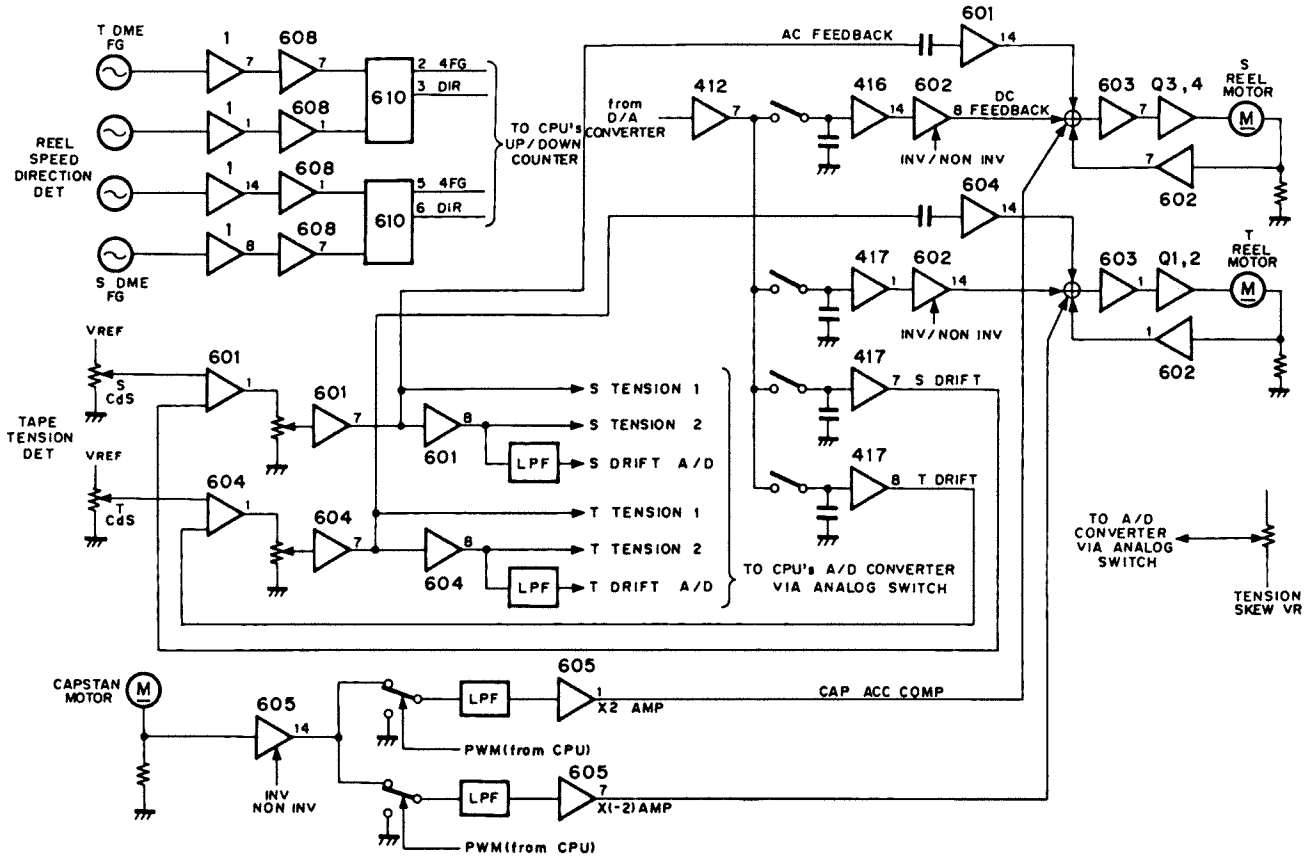


Fig.4-24. Hardware Configuration of Reel Servo

4-14. EACH REEL SERVO SYSTEM

During the pinch roller is pressed against the capstan, the tape tension between the take-up side and supply side is separated. Consequently, the VTR operation modes are broadly divided into those when the pinch roller is pressed against the capstan and those when it is not pressed against the capstan.
The reel servo operations are described in the sequence indicated in Fig.4-25.

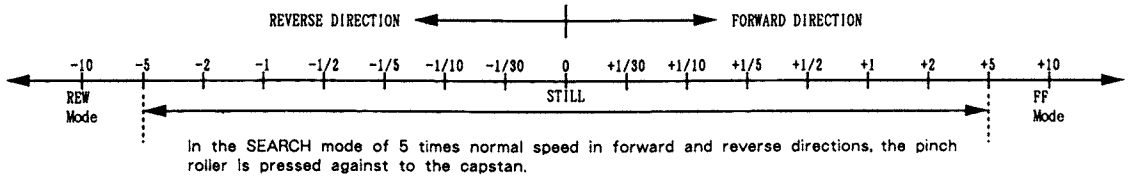


Fig.4-25.

1. Reel Servo in Search Mode

In the search mode, the pinch roller is pressed against the capstan at all times with all tape speeds ranging from FWD +5 times through STILL to REV −5 times normal speed. The tape speed during this time is determined by the capstan motor rotation.
While the pinch roller is pressed against the capstan, the control for the supply and take-up reel motors are separated. The reel servo controls the torque at the T and S side motors by the information from calculated tape diameter and tension detecters so that both sides motors keep a constant torque. During this time, the speed servo function is not used. The objective of the tension servo in this mode is to attain a tape tension with remains stable at all times at both the take-up and supply sides.
In the normal playback mode, the pinch roller is also pressed against the capstan and so the tape speed is determined by the rotational speed of the capstan.

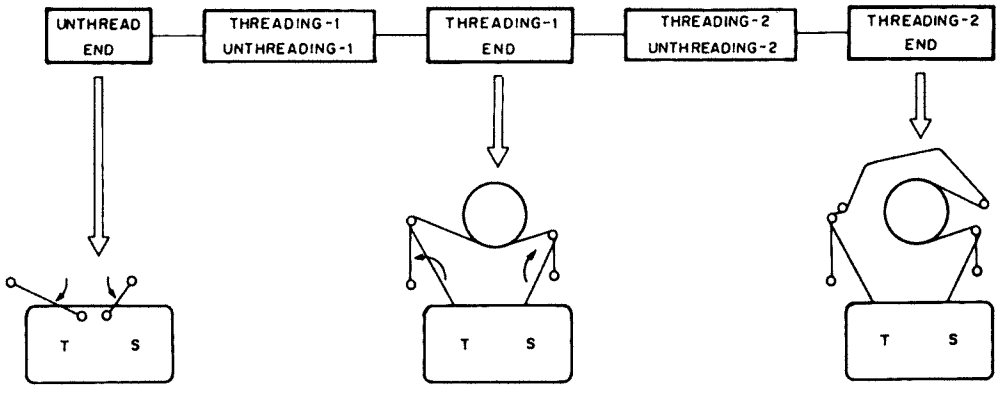
2. Reel Servo in Stop Mode

Even in the stop mode, the pinch roller is pressed against the capstan, so the capstan motor is in stop servo mode and the reel servo is in the same mode as search still.

CONDITION OF MECHANISM (See below illustration)	OPERATION MODE OF VTR	OPERATION OF REEL SERVO		DESCRIPTION	PINCH ON
		T-REEL MOTOR	S-REEL MOTOR		
STATE OF THREADING-2 END	1. SEARCH { FWD 5× ↑ STILL ↓ REV 5×	Tension servo		T and S tape tensions are separated by the capstan and pinch roller.	○
	2. NORMAL PB				○
	3. STOP				○
	4. FAST FORWARD	Tension servo and speed servo		Tape is threaded around the drum. Note. 1	×
	5. REWIND	Tension servo and speed servo		Tape is threaded around the drum. Note. 1	×
	6. STANDBY OFF	Motor off and mechanical brake		Slack the tape around the drum and stop the drum.	×
	7. BRAKING	Tension servo and speed servo			×
PERIOD BETWEEN THREADING-2 AND UNTHREAD END	8. THREADING-1 PERIOD	Torque drive	Mecha. brake		×
	9. THREADING-2 PERIOD	Tension servo	Mecha. brake		×
	10. UNTHREADING-1 PERIOD	Torque drive	Mecha. brake		×
	11. UNTHREADING-2 PERIOD	Tension servo	Mecha. brake		

Note 1. Tape is threaded immediately after the cassette tape is inserted into the VTR when the semitransparent tape is not detected.
2. When the leader or trailer tape is detected during the threading, the VTR will go into the short-FF or short-rewind mode and the mechanical brake shoe is applied for braking.
3. A mechanical brake system works when the VTR is in the threading, unthreading, standby, tape protection operation or power-off conditions. Mechanical brake system is not used during the normal operation.
4. Name of mechanism condition :

Table 4-1.



3. Reel Servo in FF and REW Modes

The "modes in which the pinch roller is pressed against the capstan" include such important operations as recording and playback. The fast forward and rewind modes are other important operations.

An outline of the reel servo operations for the fast forward and rewind modes is given below.

In the fast forward and rewind modes, the pinch roller is released from the capstan and the tape travels at high speed while threaded around the drum so that the tape access can be speeded up and the editing time reduced. Although a high tension is applied to the tape and the tape may be pulled at high speed in order to conduct high-speed fast forwarding or rewinding, the physical properties of the tape impose a ceiling on the tape. When this ceiling is exceeded, the tape is damaged. Consequently, the tape tension is detected at all times and at the same time the tape is pulled by the proper torque.

A high friction coefficient in the VTR tape transport leads to increase the tape tension, and so this prompted improvements in the transport system mechanism.

The threading angle for the stationary guide of the tape was reduced and the stationary guide was changed to a roller type. In the BVU-800 series, the supply side reel applied the servo to attain a constant reel table rotation speed and so the tape speed differed according to the position of the tape. In contrast, the BVU-950 features a servo which results in the attainment of a constant tape. speed. Furthermore, a microcomputer detects the tape diameter on the reel table in order to compensate the inertia and it increases the tape speed at the starting point of fast forward and rewind so that the amount of time taken for fast forwarding is less than that of the BVU-800.

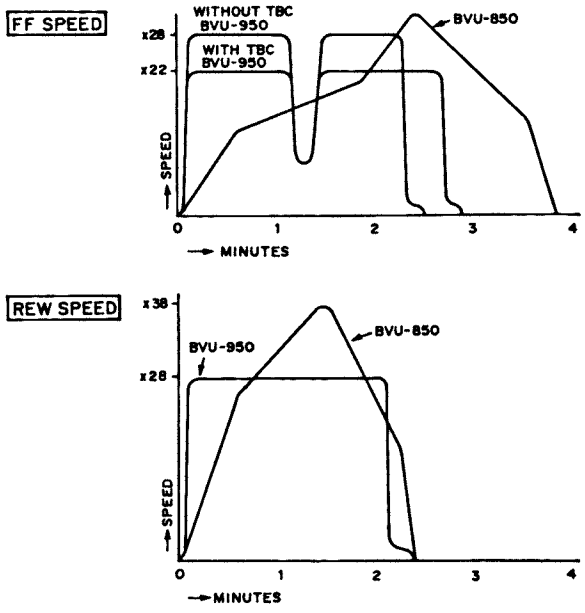


Fig.4-26. FF and REW Speed

The tape speed in the FF/REW/×10/BRAKE modes are controlled by the reel servo system. Reel servo controls the tape tension of the take-up and supply reels with tape diameter detector and tension detector. Tape speed is controlled by varing the take-up and supply tensions.

4. Reel servo in standby mode

In the standby mode, the signal voltage is not sent to the reel motors and only the mechanical brake is applied to the take-up and supply reel tables. As a result, the tape tension is not stabilized and the tape threaded on the head drum becomes slack. The drum also stops rotating.

5. Reel Servo in Threading-1 Period

The threading-1 period as shown in the Table 4-1 is the operation of pulling the tape out of the cassette casing as far as the threading-1 end position using an arm, after the cassette tape has been loaded into the VTR.

As indicated in Table 4-1, to thread the tape, braking is applied to the supply reel table which is then fixed, and the back-tension torque is applied to the take-up reel table. During threading, therefore, the tape is supplied from the take-up side.

6. Reel Servo in Threading-2 Period

The threading-2 period means that the rotating the threading ring from the threading-1 end position, threading the tape onto the head drum and the pinch roller is positioned in front of the capstan.

The supply reel table in the threading-2 period is fixed by mechanical braking as in the threading-1 period. The take-up reel table is given a torque of 40 grams tension.

During the threading-2 mode, therefore, the tape is supplied from the take-up side, as in the threading 1 period.

7. Reel Servo in Unthreading-1 and 2 Periods

In the unthreading modes, the mechanical brake is applied to the supply reel table and the tape is returned to the take-up reel.

4-15. TENSION DETECTOR

The objective of the tension detector is to amplify the CdS output signal and add a voltage for correcting the zero point of the CdS output signal automatically.
Since the same circuitry is featured for both the take-up and supply sides, the description here is confined to the supply side.
The tension detector outputs of both the take-up and supply sides are first supplied to the zero point adjustment circuit on the SV-88 board.
The voltages output by the tension detectors will vary a little in accordance with changes in the temperature and with aging. Since it is thus not possible to detect the zero-tension properly, these fluctuations are corrected by the automatic zero point adjustment circuit.
The automatic zero point adjustment is undertaken by the operational amplifier IC601 and the microcomputer. The BVU-950 uses the microcomputer to detect the correction voltage accurately across a wide range.
The supply side CdS output is supplied to pin 3 of operational amplifier IC601 from pin 26B of CN1 on the SV-88 board. The correction voltage used to adjust the zero point from the microcomputer is fed back negatively to pin 2 of IC601.
The pin 1 of IC601 output is supplied to pin 10 of the same IC through RV601, it is amplified for 4 times, it passes through the multiplexer IC403 on the SV-88 board and it is input to pin 35 of the microcomputer's analog input port IC407.
The microcomputer reads out the voltage when the tape tension is not applied and it outputs the corrected data. These data are D/A converted and, through feedback to pin 2 of IC601 on the SV-88 board, the pin 1 of IC601 output is automatically adjusted to 0V DC with a tension of 0 grams.
If the LED for the tension detector is disconnected for some reason or other, this is detected at pins 8, 9 and 10 of OR gate IC115, and the tape is protected.

4-16. REEL FG DETECTOR

The DME output of approximately 100mVp-p from the take-up and supply sides is amplified by the FG amplifier on the SE-48 board and it is then input to the SV-88 board. The FG signal is adjusted by the variable resistor on the SE-48 board so that the duty cycle of the IC608 and IC609 output pulse width is set to 50%. The 4FG and direction signals are then both output by IC610. Q612 is a 7.5V regulator which serves to eliminate the noise in the power supply of the FG amplifier.

4-17. REEL ERROR DETECTOR

Once the CdS output has been adjusted to zero point and output from pin 1 of IC601, it is supplied to the buffer and amplifier inside the IC601.
A two-stage tension detector is provided to change the scale used in accordance with the differences in the tape tension applying during playback and fast forwarding. A DC voltage of 1.0V can be monitored at TP601 with a tension of 100 grams and a voltage of 4.0V can be monitored at TP602 with a tension of 100 grams.
This data is detected by the microcomputer at an 8-bit resolution (256 stages). When the tension is less than 125 grams, 1 bit is processed using the 0.5 gram information and when it is more than 125 grams, it is processed using the 2 gram information. Using the speed and other such information from the system controller, the microcomputer feeds back the AC and DC components with the target value and adds the reel error to the motor. The microcomputer now calculates and outputs the tape threading diameter and reel inertia.
The DC components of the reel servo error are processed inside the microcomputer using the tension detection output and reel FG signals, and it is output from the microcomputer as the S-TORQUE DA OUT signal. The S-TORQUE DA OUT signal is supplied to pin 9 of IC602 on the SV-88 board.
Depending on the direction signal supplied to the base of Q607, a positive or negative voltage is output from pin 8 of IC602. This makes the motor generate the torque in the forward or reverse direction. The AC components from the tension detector are fed back to pin 14 of IC601 and mixed with the DC components.
The switcher IC606 serves to select the AC feedback gain according to the size of the cassette. The gain is increased with the KCA cassette.
The moment of inertia of the reel motor is compensated by IC605 and IC607 on the SV-88 board. A voltage, which is proportionate to the drive torque of the capstan motor, is input to pin 13 of IC605. A PWM signal from the microcomputer corresponding to the reel's moment of inertia is input to pin 10 of the switcher IC607. A voltage corresponding to the acceleration or deceleration of capstan is generated and applied to the reel motors to compensate the reel inertia.

4-18. REEL DRIVE CIRCUIT

The reel error information input to pin 6 of IC603 drives the reel motor. At this time, a voltage proportionate to the reel torque is fed back to pins 5 and 6 of IC602, and IC603 drives the motor at a constant torque.
The drive current of the supply reel motor is input to pins 5 and 6 of IC602 on the SV-88 board after the voltage has been detected by R4 on the DR-53 board and the current sensitivity has been adjusted by RV2. A DC voltage of 1V is produced at TP611 when the reel torque is 500 grams.

4-19. CTL CIRCUIT

The objective of this circuit during recording is to supply the CTL recording current to the CTL head, and during playback it is to amplify the playback CTL signal from the CTL head and shape it into a rectangular waveform.

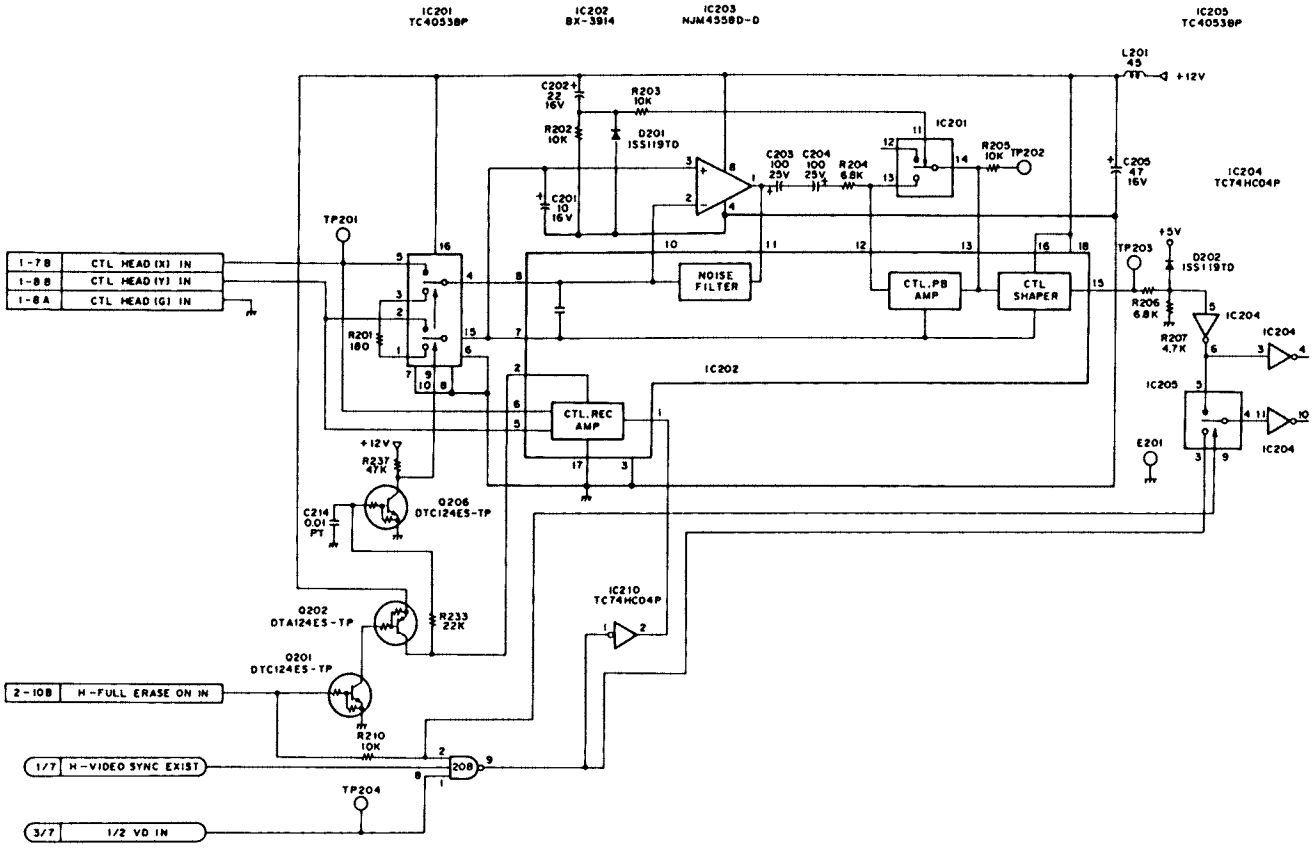


Fig.4-27. CTL Amplifier

4-19-1. CTL Amplifier and Waveform Shaper (IC202, 203)

The CTL head (X) and (Y) signals arrive from both ends of the CTL head winding, and they are supplied to IC202 and IC203 via the switcher IC201. IC203 is the first stage amplifier ; the bias and feedback circuits are located inside IC202. The signals are then supplied to the inverting amplifier inside IC202 via the coupling capacitors C203 and C204, and the output is shaped by the Schmitt trigger inside IC202 and output to pin 15 of IC202.

4-19-2. REC/PB Selector

During recording, Q201 and Q202 supplies a 12V voltage to pin 2 of REC amplifier power supply IC202.
The pin 1 and 3 of switcher IC201 shortcircuits the input pins of the playback amplifier, which has been isolated from the head during recording, using a 180 ohm dummy resistor. This resistance is roughly equal to the resistance of the head. As a result, the offset voltage fluctuations of the IC203 output are kept to the minimum during recording-to-playback transition by means of the IC203 input offset current, and the playback amplifier bias is stablized momentarily at recording-to-playback point.
If this circuit were not present, the gain of IC203 would be high and so the DC components at the output voltage would differ during recording and during playback due to the different input resistance of IC203. Therefore, when the mode is switched from recording to playback, the next stage coupling capacitor charges and discharges. If the next stage becomes saturated (this is, in other words, the worst possible circumstance), it will not be possible to amplify the CTL signal properly for at least 10 seconds.
Even when the mode is switched from recording to playback, this circuit enables the proper CTL waveforms to be output quickly.

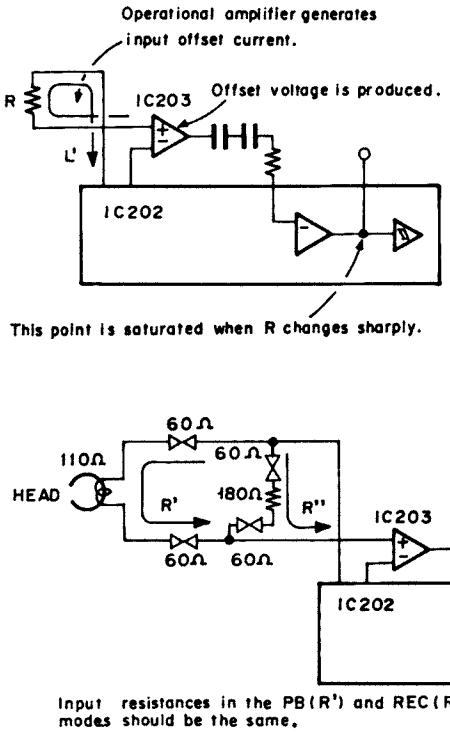


Fig.4-28. REC/PB Selector

4-19-3. Power ON Reset Circuit

When the power switch on the BVU-950 is turned on, the loaded tape is unloaded and the reel servo bias is automatically adjusted, the tape is loaded again and the mode is switched to play or stop.
If the CTL playback amplifier is stabilized within the loading time (at least 4 sec), the CTL signal can be played back without any omission.
When the power is turned on, a voltage differing from that during the playback operation is charged in C203 and C204. This saturates the second stage amplifier inside IC202 and makes it impossible to play back the CTL signal properly.
In order to stabilize C203 and C204, their load must be discharged through R204 and R_B. The voltage applying during the playback operation in C203 and C204 is : (IC203 output offset voltage − V_R).
If the switch in Fig.4-29 is set to on, the input impedance of the IC202 second stage amplifier as seen from C204 will be virtually zero. This is because the second stage amplifier becomes a voltage follower whose input is V_R. Immediately after power is switched on, C202 and R202 will go ON in approximately 0.2 sec. This means that, in the circuit shown in Fig.4-29, the playback amplifier will be functioning properly in 0.5 sec. after the power has been turned on.

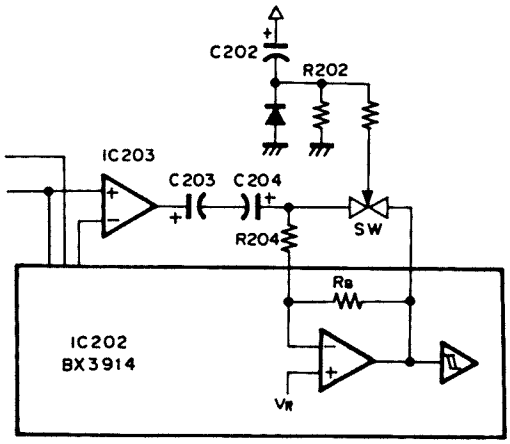


Fig.4-29. Power ON Reset Circuit

4-19-4. CTL Compensator

When the direction of the tape transport in the VTR is suddenly changed from forward to reverse or when the tape speed is rapidly changed, there is a possibility that the CTL playback circuit will cause an error.

In order to safeguard against this, the editing precision is enhanced by using the capstan FG signal to compensate for the CTL signal.

The CTL compensator is composed of IC211, IC214, IC213 and IC219 which is consisted of FG counter and a microcomputer for CTL compensation. The microcomputer controls set and preset of the FG counter so that it outputs a FG-compensated CTL signal which is equivalent to the playback CTL. The microcomputer also controls the muting of FG-compensated CTL when a CTL is not recorded on the tape.

SECTION 5
SYSTEM CONTROL BLOCK

5-1. OUTLINE

The system control block of the BVU-950 is composed of the SY-102, KY-101 and BC-11 boards.
Microcomputers provide distributed processing for each block and, through the adoption of serial communication with the various blocks, it has been possible to reduce the amount of space taken up by the parts (by introducing single-sided circuit board). As shown in Fig.5-1, the overall configuration of the system block is centered on the main CPU which is mounted on the SY-102 board. This CPU communicates with and controls the various microcomputers, time codes, and 9-pin/24-pin interface circuitry. In addition, microcomputer M2 serves to control the mechanism and communicate with the SV and AV microcomputers. The functions and operations of each microcomputers employed in the BVU-950 will be described as follows.

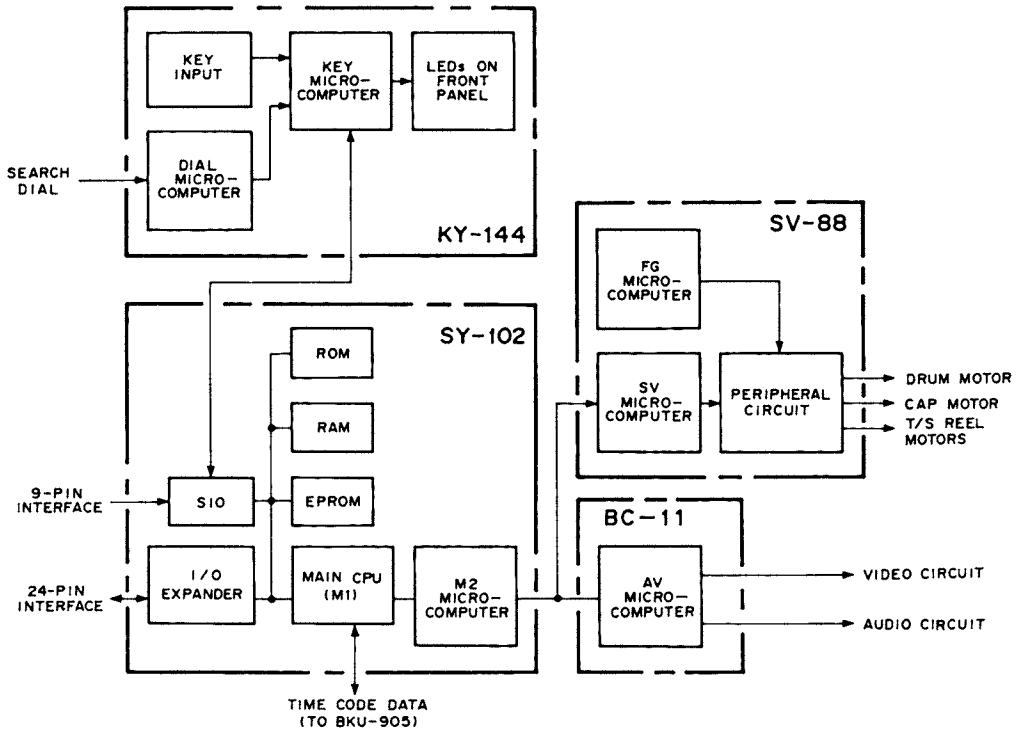


Fig.5-1. System Control Block Diagram

5-1-1. Microcomputer M1 : IC1/SY-102 (TMPZ84C011AF)

The M1 is an 8-bit single-chip microcomputer with a 100-pin flat pack configuration. It is characterized by its large number of I/O ports including the counter timer and clock generator.
Configured in this microcomputer are a Z80 CPU, clock generator, CTCs for 4 channels, and five parallel input/output ports (PIO : PA through PD).
The M1 is the main CPU in the system control circuitry and through the data bus it serves to control the RAM, ROM, SIO, I/O expander, and time code reader/generator. Through the SIO, microcomputer M1 also provides 9-pin remote communication and communication with the KY microcomputer, while through the I/O expander, it provides 24-pin parallel communication. Through microcomputer M2, it provides communication with the SV microcomputer and AV microcomputer, and the M1 and M2 microcomputers communicate through the respective parallel I/O ports.

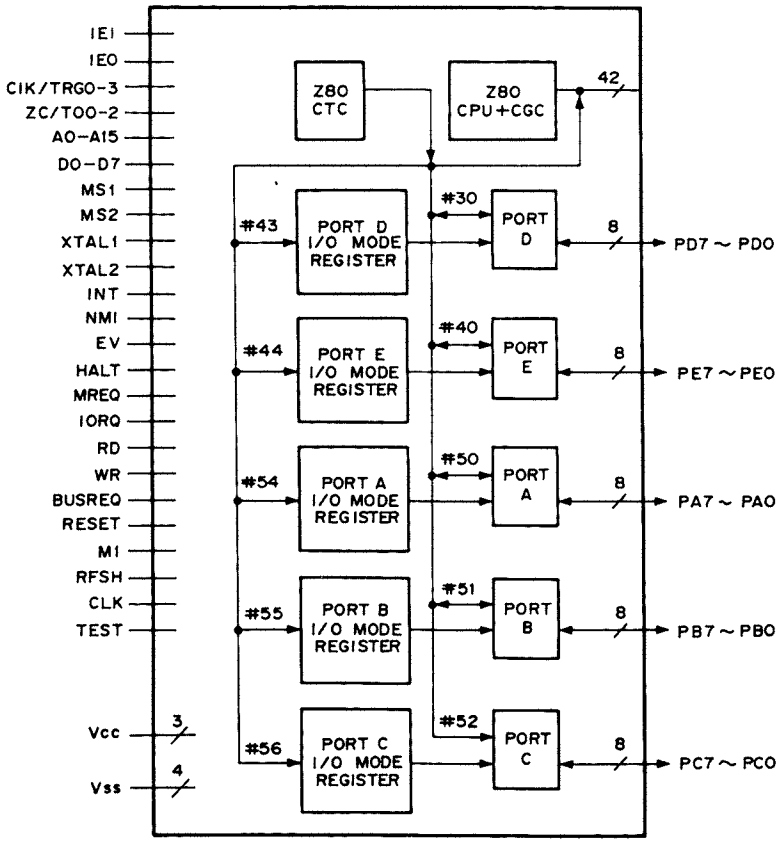


Fig.5-2. Microcomputer M1

5-1-2. Microcomputer M2 : IC7/SY-102 (MB88551H)

The M2 is a 4-bit single-chip microcomputer whose main purpose is to input the mechanism and sensor information in order to control the solenoids, motors and other mechanisms. Through parallel communication with microcomputer M1, it communicates with the SV and AV microcomputers.

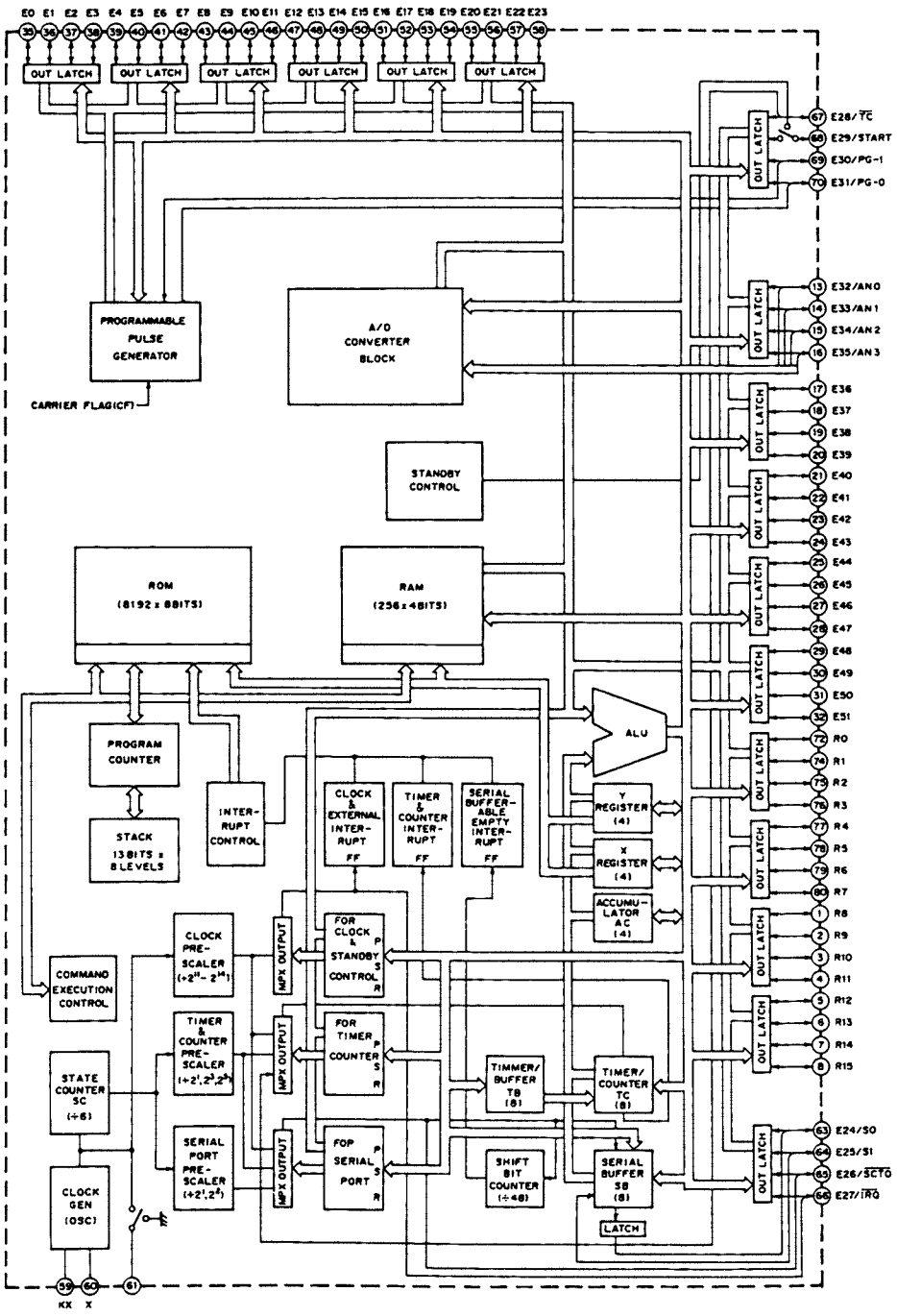


Fig.5-3. Microcomputer M2

5-1-3. KY Microcomputer : IC1/KY-101 (M50747H)

The KY is an 8-bit single-chip microcomputer. It controls the function keys on the front panel, the LEDs and the 7-segment LEDs (timer display), and it serves as an hours meter.
Instead of an hours meter composed of a mercury clock as used in the conventional BVU, the BVU-950 employs a digital hours meter based on a microcomputer.

5-1-4. Dial Microcomputer : IC7/KY-101 (MB88201H)

The dial microcomputer is a 4-bit microcomputer. It processes the data of the search dial on the front panel and sends these data to the KY microcomputer.

5-1-5. SV Microcomputer : IC407/SV-88 (μPD78310)

A servo LSI (CX194) is employed for the drum and capstan servos in the BVU-800 series and the reel servo is composed of analog circuitry.
In the BVU-950, however, the drum, capstan and reel servo circuits are controlled by the SV microcomputer. The SV microcomputer communicates with the main CPU (M1) through microcomputer M2, and so only the aspect of communication between microcomputer SV and microcomputer M2 will be described here. For further details on the SV microcomputer itself, reference should be made to the description of the servo system.

5-1-6. AV Microcomputer : IC401/BC-11 (MB88525)

The AV microcomputer is a 4-bit single-chip microcomputer. As with the SV microcomputer, it communicates with the main CPU (M1) through microcomputer M2.
The main functions of microcomputer AV are to control the commands, which are sent to the audio and video circuits, and to control the recording/playback amplifier circuit for the time code on the BC-11 board.

5-2. SY-102 BOARD

5-2-1. Main CPU (M1)

1. CTC Circuit

Pins 5 through 2 of IC1 are the clock/trigger input terminal of the 4-channel CTCs inside microcomputer M1.

- CTC channel 0 input (IC1 pin 5) :
  The 1/2 VD signal from the servo circuit is supplied to this pin and used as the timing clock pulse of the system control circuit.
- CTC channel 1 input (IC1 pin 4) :
  The TC INT signal is supplied to this pin, the interrupt is applied by this signal to microcomputer M1 and the time code data are read into microcomputer M1.
- CTC channel 2 input (IC1 pin 3) :
  The EDIT CTL signal is supplied to this pin. The EDIT CTL signal which has been compensated for by the capstan FG signal in the servo circuit and the number of CTL pulses are counted by the CTC inside microcomputer M1. The up/down control of the CTL counter is switched by the TAPE DIRECTION (H : FWD) signal which is supplied to pin 94 of IC1. A change in the tape direction is detected by the NMI detector composed of IC9, 10, 11 and 13, an interrupt is applied to microcomputer M1 which is advised that the tape direction has been inverted.
- CTC channel 3 :
  This is used as the timer for the 9-pin connector remote communication.

2. PD Ports

The PD ports (PD1 through 7) are the input ports and the following signals are supplied.

- PD1 (IC1 pin 95) : H=NTSC, L=CCIR system select
- PD2 (IC1 pin 94) : TAPE DIRECTION (H=FWD, L=REV)
  Up/down control for the CTL counter.
- PD3 (IC1 pin 93) : TC CONNECTION
  Low when the time code generator/reader board (BVU-905) is connected.
- PD4 (IC1 pin 92) : TAPE DIRECTION
  This signal is used for announcing the tape direction in the NMI interrupting condition when the direction of the CTL will be changed.
- PD5 (IC1 pin 91) : 1/2 VD
  This signal is used to interrupt the M1 at the rising and falling edges. Also used for controlling the communication timing of KY, 9-PIN and M2 microcomputers.
- PD6 (IC1 pin 89) : REMOTE 1 (L=pin 9/H=pin 24)
  This signal is supplied from the 9-pin/24-pin remote communication selector switch below the front panel. It is effective only when the REMOTE 2 signal below is in the REMOTE states, and it selects either the 9-pin or 24-pin connector.
- PD7 (IC1 pin 88) : REMOTE 2 (L=REMOTE/H=LOCAL)
  The signal from the REMOTE/LOCAL switch on the front panel is input.

3. PB Ports (PB0 to 7),PE Ports (PE0 to 7)

The PB ports and PE ports provide interfacing with the time code board (BKU-905). The TC DATA 0 through 7 are written into the BKU-905 or read from the BKU-905 by the TC ADDRESS 0 through 7 and RD or WR signals.
The time code data on the data bus line are read out, the preset TC circuit mode is controlled and the character generator data are set.

4. PC Ports

The PC ports are used for output ports and the following signals are output.

- PC0 (IC1 pin 60) : STROBE 0
  The $\overline{\text{STB 0}}$ signal is the strobe signal which is sent to microcomputer M2 from microcomputer M1 during communication between these two microcomputers.
- PC1 (IC1 pin 59) : DATA IN/$\overline{\text{OUT}}$
  This signal indicates the direction of data during communication between microcomputer M1 and microcomputer M2.
- PC2 (IC1 pin 58) : L=NON-VOL RAM RECALL
  This is the control line for reading out the data from the non-volatile RAM IC4.
- PC3 (IC1 pin 57) : L=NON-VOL RAM STORE
  This is the control line for storing the data in the non-volatile RAM IC4.
- PC4 (IC1 pin 56) : L=I/O EXPANDER RESET
  This signal is for resetting the I/O port expander IC6.
- PC5 (IC1 pin 55) : H=NMI ENABLE
  This signal selects whether to provide the NMI (non-maskable interrupt).
- PC6 (IC1 pin 54) : COMMUNICATE DIRECTION A
- PC7 (IC1 pin 53) : COMMUNICATE DIRECTION B
  The COMM DIR A and B signals determine the 9-pin connector remote communication mode. By controlling the RS-422 driver IC12, this unit is operated as the master or slave.

COMM DIR A (IC1-54)	0	1	0	1
COMM DIR B (IC1-53)	0	0	1	1
IN (IC5-12)	①&②	③&④	①&②	③&④
OUT (IC5-15)	③&④	③&④	①&②	①&②
MODE	SLAVE	MONITOR	MONITOR	MASTER

NOTE: ①, ②, ③ and ④ in the table denote signals ①, ②, ③ and ④ of the 9-PIN interface signal.

Table 5-1. Communication Direction

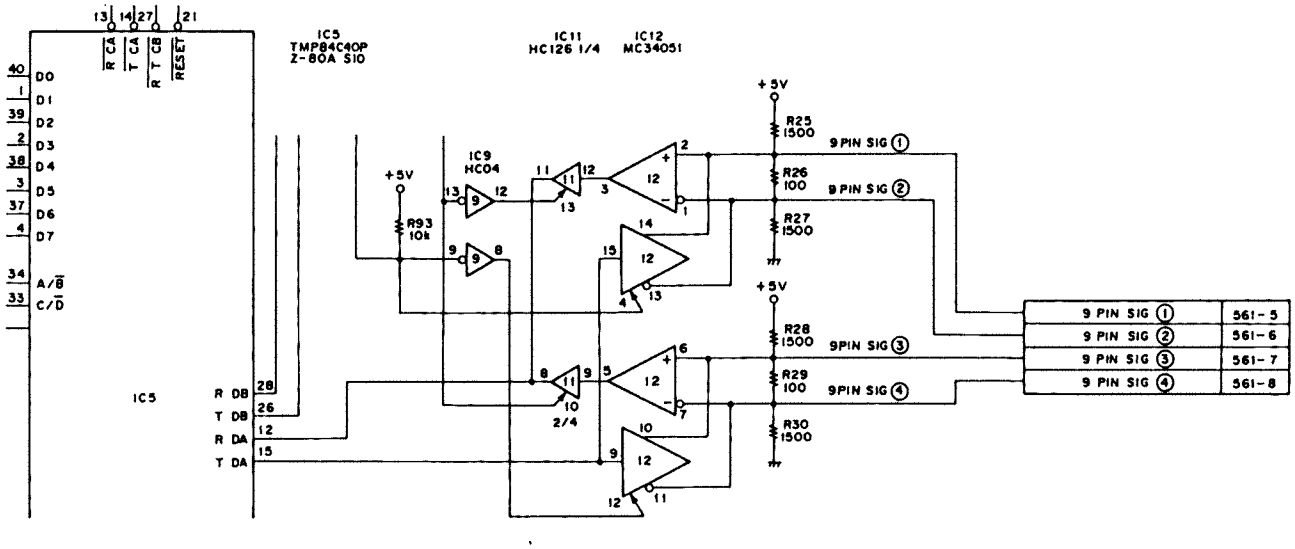


Fig.5-4. RS-422 Driver

5-2-2. Peripheral Circuits of Main CPU (M1)

1. Memory (IC2, 3, 4)

IC2 is a 32K bytes ROM and IC3 is an 8K bytes RAM, and each is controlled by the main CPU. IC4 is a non-volatile RAM.

Conventional VTRs used a large number of DIP switches in the system control and other such circuits for the mode settings. In contrast, the BVU-950 stores the mode information in the non-volatile memory IC4 which plays the role of these switches. This non-volatile RAM has a 256-byte memory capacity which is equivalent to 256 4-bit DIP switches. Fig.5-5 shows a memory map of the ROM, RAM and non-volatile RAM.

Pins 17, 18, 19 and 20 of IC1 output the MEMORY REQUEST, I/O REQUEST, READ and WRITE signals respectively to the memory and I/O circuit where they read or write the data.

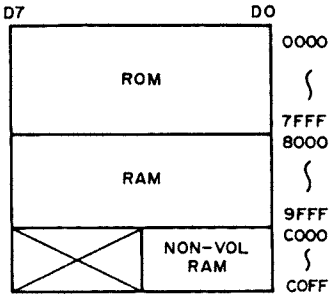


Fig.5-5. Memory Map

2. SIO (IC5)

The SIO IC5 is the controller for serial communication and it contains 2-channel input/output circuit. One channel is used for the 9-pin connector remote communication and the other channel is for communication with microcomputer KY mounted on the KY-101 board. Used as the clock signal for serial communication is the 614kHz signal which is generated by the oscillator composed of X1 and IC10. Channel A of SIO IC5 provides the 9-pin connector remote communication through the driver/receiver IC12 at a transfer rate of 38.4kbps. Channel B of SIO provides communication with the microcomputer KY through the interface circuit composed of Q5 and Q6 at a transfer rate of 19.2kbps.

3. I/O Expander (IC6)

IC6 is an I/O port expander for IC1 main CPU (M1), and it provides communication with the 24-pin parallel remote control.

The PB ports (PB0 through 6) of IC6 are ports for the command inputs from the external remote controller and the PA ports (PA0 through 6) are ports for the VTR status outputs vis-a-vis the commands. The PC and PD ports are not used in the BVU-950. Tables 5-2, 5-3 and 5-4 show the interface specifications of the 24-pin connector.

Ports PX0 through 3 of IC6 are signals for controlling the BKU-905.

- PX0 (IC6 pin 49) : CNT 0
- PX1 (IC6 pin 50) : CNT 1
  These two signals are sent to the character generator in the BKU-905 to control the register inside this generator.
- PX2 (IC6 pin 52) : CNT 2
  Parallel output signals for servo system (not in use)
- PX3 (IC6 pin 53) : CNT 3
  The low level of TC RD signal is output from this pin which is low when the time code data are read from the BKU-905 and when the mode of time code circuit is detected.

ITEM	DESCRIPTION
POINTS	• 9-pin connector is standard for editing. • 24-pin new GPI connector is simple parallel remote control for system up by user.
PURPOSE	• Timer Rec Control • Multi Start Control on Multi Dubbing • Auto Start
OPERATION	• FF/REW/REC/PLAY/STOP/ STANDBY (COMMAND & STATUS) • EJECT (COMMAND) • CASSETTE IN (STATUS) • POWER (+5V) • GND • SPARE (8 pins)
CONNECTOR	• AMPHENOL (24 pins)

Table 5-2. 24-Pin New GPI Connector

PIN No.	I/O SIGNAL	PIN No.	I/O SIGNAL
1	+5V OUT	13	STANDBY STATUS
2	STOP COMMAND	14	CASSETTE IN STATUS
3	FF COMMAND	15	REC STATUS
4	PLAY COMMAND	16	SPARE
5	REW COMMAND	17	SPARE
6	STANDBY COMMAND	18	SPARE
7	EJECT COMMAND	19	SPARE
8	REC COMMAND	20	SPARE
9	STOP STATUS	21	SPARE
10	FF STATUS	22	SPARE
11	PLAY STATUS	23	SPARE
12	REW STATUS	24	GND

Table 5-3. 24-Pin New Simple Parallel Remote Control

Specifications

(1) Timing
Command Pulse Width·····A≧50msec
Status Response·····B≦50msec

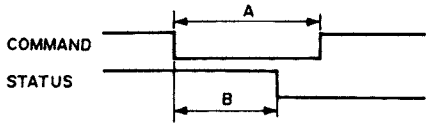


Fig.5-6. 24-Pin Signal Timing Format

(2) Polarity
Command·····Active "Low"
Status·····Active "High"

(3) I/O

STATUS OUTPUT	LS-TTL Level (Compatible)	L : Less Than 0.8V H : More Than 2.7V SINK CURRENT : Less Than 8mA
COMMAND INPUT	C-MOS Level (Compatible) (4.7k Ω PULL-UP)	L : Less Than 1.5V H : More Than 3.5V

Table 5-4. Contents of I/O Status and Command

(4) +5V Output
5±0.5V/100mA (max.)

4. Reset Circuit

This circuit is composed of IC8, IC9, Q2, Q3 and Q4. It detects the following three reset conditions.

- Power ON Reset
  Resetting is accomplished when the power is switched on by driving Q4 into conduction during the R8 and 9 and C11 time constant.
- Supply Voltage Drop Detection
  When the supply voltage drops momentarily, some circuits will continue to function normally while other will not. To cope with situations like this, the microcomputer is reset and operation is started after the supply voltage has stabilized sufficiently. Q2 detects the drops in this voltage.
- Microcomputer Malfunction Detection
  The M1 and M2 microcomputers are communicating at all times in the vertical period. Consequently, the STROBE pulse is output at all times, but when something interferes with the communication between these microcomputers, this is treated as a run-away in the software and the microcomputers are reset.
  The STROBE 1 signal that is output from pin 96 IC1 is input to the monostable multivibrator IC8. If it is found to be missing for approximately 100msec or longer, a high-level signal is output from pin 12 of IC8 and the microcomputers are reset.

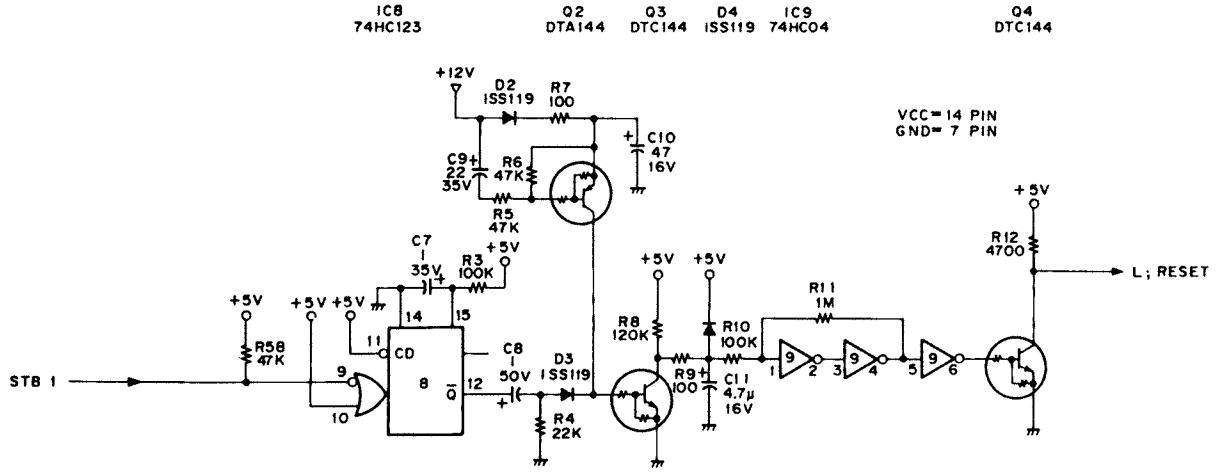


Fig.5-7. Reset Circuit

5-2-3. Microcomputer M2 and Peripheral Circuits

The microcomputer M2 (IC7) serves to communicate with the M1, SV and AV microcomputers. It also supply the information from the sensors, photo-interruptors and switches on the front panel to the other microcomputers, and exercise control over the two motors and three solenoids.
The signals input to, and output from, microcomputer M2 are as follows.

- E11 (IC7 pin 46) : MISS REC (L=RECORDING ENABLE)
- E12 (IC7 pin 47) : THREAD END 1
- E13 (IC7 pin 48) : THREAD END 2

TH END-1	TH END-2	RING POSITION
1	1	CASSETTE IN↔THREAD END-1
1	0	THREAD END-1 (=FR STOP)
0	0	THREAD END-1↔THREAD END-2
0	1	THREAD END-2

Table 5-5. Ring Position

- E15(IC7 pin 50): L=SP TAPE/H=CONVENTIONAL TAPE
- E27 (IC7 pin 66) : 4VD (IREQ)
  The microcomputer M2 is interrupted by the 4VD signal. The 4VD signal is the reference signal for the microcomputer M2 processing.

- E10 (IC7 pin 45) : L=DEW DETECT

Dew (Condensation) Detector Block
A IC15 is an oscillator. When no dew is detected, a high level of negative feedback is applied by R37 and no oscillation results. When dew is detected, one side of C24 is connected to ground, the negative feedback applied by R37 is reduced and oscillation begins. Q7 is driven into conduction by the signal produced by smoothing the resulting output, which is detected by D9 and 10, using C28.

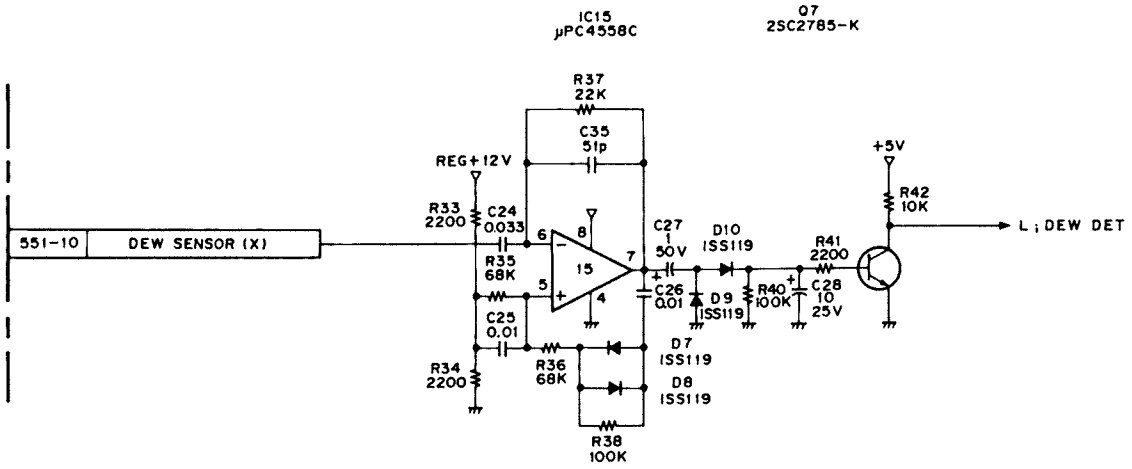


Fig.5-8. Dew (Condensation) Detector

• E9 (IC7 pin 44) : L=TAPE END
• E8 (IC7 pin 43) : L=TAPE TOP

Tape Top and Tape End Detector

IC16 and Q8 configure the tape top/tape end detector. Reference voltages of approximately 8.9V and 3.1V are supplied respectively to pins 5 and 2 of IC16.

When the tape end is detected

The voltage at TP3 becomes approximately 11V, pin 7 of IC16 is set to low level and pin 1 of IC16 is set to high level. When the tape end is detected, the VTR enters the rewind mode.

When the tape top is detected

The voltage at TP3 becomes approximately 0.1V, pin 7 of IC16 is set to high level and pin 1 of IC16 is set to low level. When the tape top is detected, the VTR is set to the SHORT FF (fast forward) mode, and after the tape has been rewound completely, the VTR enters the stop mode.

When both sensor are not detected (Normal status)

The voltage at TP3 becomes approximately 6V, pin 7 of IC16 is set to high level and pin 1 of IC16 is also set to high level.

When both sensors are detected

The voltage at TP3 becomes approximately 6V, pin 7 of IC16 is set to high level and pin 1 of IC16 is also set to high level, which is the same as for the normal status. However, Q8 is forcibly turned on and the tape top is detected.

(1) When the leader tape is detected by both sensors at the tape top section, the VTR enters the SHORT FF mode.
(2) When the trailer tape is detected by both sensors at the tape end section, the VTR enters the SHORT FF mode, the stopping of the reel is detected at the final tape position, and the VTR enters the stop mode.

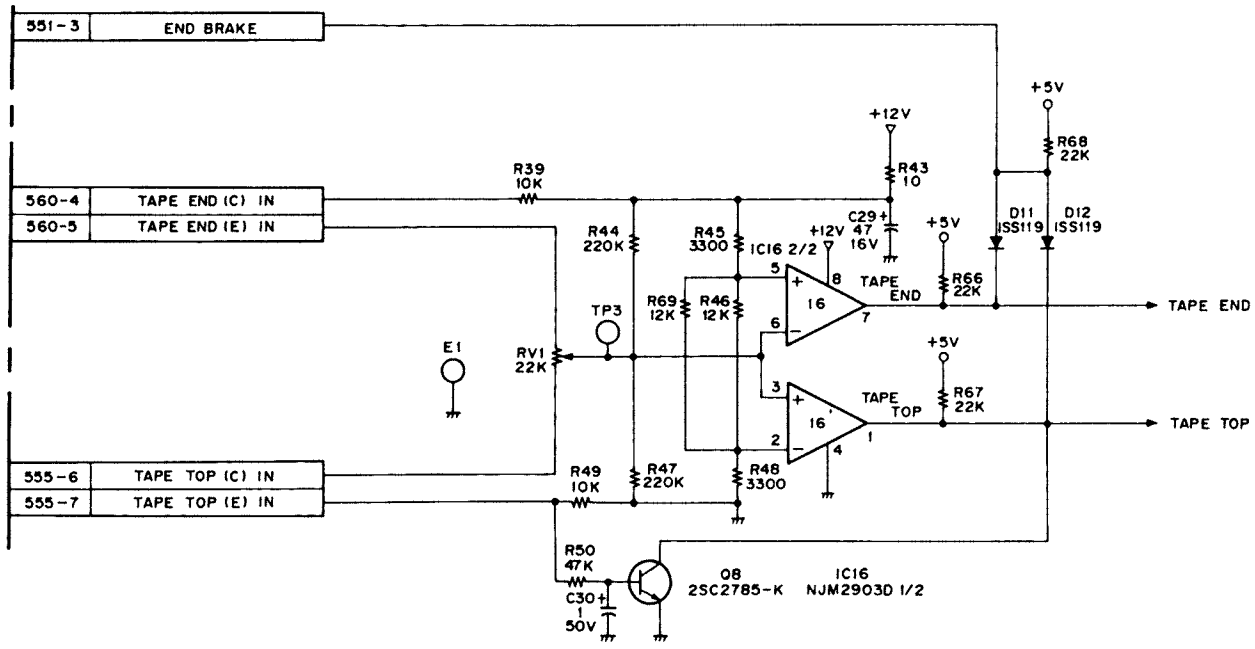


Fig.5-9. Tape Top/End detector

- E20 (IC7 pin 55) : H=CASSETTE IN
- E21 (IC7 pin 56) : H=CASSETTE DOWN

H : C IN	H : C DOWN	CASSETTE POSITION
0	1	CASSETTE UP COMPLETION
0	0	CASSETTE IN
1	0	CASSETTE IN↔CASSETTE DOWN
1	1	CASSETTE DOWN COMPLETION

Table 5-6. Cassette Position

- E22 (IC7 pin 57) : H=UNTHREAD END
  This is set to high level when the drawer arms at the take-up and supply sides return inside the cassette.
- E23 (IC7 pin 58) : L=CASSE-COM CONNECT
  A low level signal is input when the cassette compartment is connected, however, it is not used.
- E45 (IC7 pin 26) : H=CASSE-COM LAMP
  The LED inside the cassette compartment is lit when it is high level. When the power is turned on, microcomputer M2 is reset and high level signals are output from the ports, so that the LED will light momentarily. This is prevented by D16.
- E0-E5 (IC7 pins 35 to 40) :
  The signals for the time code mode setting switches below the front panel and for the switch which determines whether characters are to be displayed or not are supplied to these pins. When the BKU-905 is not connected, they are forcibly set to the external preset mode.
- E7 (IC7 pin 42) : L=TBC MANUAL ON
  The signal from the TBC ON/AUTO switch below the front panel is input to this pin. When the low level signal is input, the unit enters the TBC ON mode at all times.
- E47 (IC7 pin 28) : DROP FRAME/NON-DROP FRAME output
  A high level signal is output when the time code is in the drop frame mode. At that time, the DROP FRAME LED below the front panel lights when Q9 is turned on.
- E16 (IC7 pin 51) : L=AUDIO LIMITER ON
- E17 (IC7 pin 52) : L=AUDIO DOLBY SWITCH ON
- E18 (IC7 pin 53) : SLACK KILLER
  By shorting this pin (TP4/SY-102) with the ground, the AUTO OFF detection by tape slack and the tape top / tape end detection are no longer performed. This facilitates VTR operational checks and adjustments.
- E19 (IC7 pin 54) : 1/2 VD
  Together with the 4VD signal, the 1/2 VD signal serves as the reference signal for the communication timing inside microcomputer M2.
- E44 (IC7 pin 25) : H=AUTO OFF
  When dew has been detected or when the low-level TAPE PROTECTION signal, which is input to pin 4 of microcomputer M2 from the servo circuit, is supplied, this output is set high and the AUTO OFF LED lights.
- E24 to E26, R12 to R15
  These signal lines are for communication with the SV and AV microcomputers.
- E36 to E39 (IC7 pins 17 to 20) :
  These signals are used to control the cassette motor and threading motor. When pins 18 and 20 are high, respectively, the motor rotates in the forward direction, the cassette is moved down and the tape is threaded.
- E40 (IC7 pin 21) : L=PINCH ON
  The timing of the low level PINCH ON output is delayed by the pinch roller ON delay circuit IC8. RV2 serves to correct any mechanical fluctuations in the stroke from pinch roller OFF to ON.

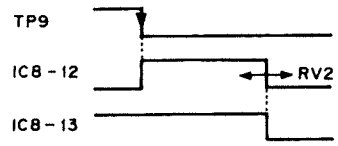


Fig.5-10. Pinch Roller ON Timing

- E41 (IC7 pin 22) : L=T-BRAKE SOL ON
- E42 (IC7 pin 23) : L=S-BRAKE SOL ON

5-3. BC-11 BOARD

The BC-11 board contains the time code recording/playback amplifier, AV microcomputer and audio erase oscillator circuit. Only the AV microcomputer will be described in this section.

The AV microcomputer functions to control the timing of the audio, video and time code recording/playback circuits, and it converts the information sent from microcomputer M2 with the actual control signals.

As far as the audio circuit is concerned, the AV microcomputer enhances the audio insert editing precision by controlling the timing while giving due consideration to the distance between the erase head and record/playback head.

As far as the video circuit is concerned, the AV microcomputer sends the recording start command prior to the edit (IN) point and so makes the video recording smooth.

5-3-1. AV Microcomputer

The input and output signals of the AV microcomputer are as follows.

- E20 to E23, P2 (IC401 pins 54 to 57, 60) : Time code recording/playback amplifier control signals
- E14 (IC401 pin 48) : L=OSC ON
- E15 (IC401 pin 49) : H=FAST TAPE SPEED
  This signal is set high in the FF, REW SEARCH ×10 and STANDBY OFF modes and it serves to attenuate the audio playback output.
- E16 (IC401 pin 50) : CHARACTER GENERATOR PB ON
- E17 (IC401 pin 51) : CHARACTER GENERATOR REC ON
  These signals determine whether characters are to be superimposed onto the video playback signals and whether the signals with characters are to be recorded during recording. These signals are latched by the 1/2 VD signal and are switched during the vertical blanking period.
- E4 to E13 (IC401 pins 38 to 47) : Audio circuit control signals
- O0 (IC401 pin 21) : H=CH-1 LIMITER ON OUT
- O1 (IC401 pin 22) : H=CH-2 LIMITER ON OUT
  The information of the audio limiter switch on the front panel is read by microcomputer M2 and controlled by these signal lines.
- O3 (IC401 pin 24) : H=CH-1 DOLBY ON OUT
- P0 (IC401 pin 58) : H=CH-2 DOLBY ON OUT
- E0 (IC401 pin 34) : L=DOLBY DET IN
- (IC401 pin 35) : L=INHIBIT IN
- (IC401 pin 36) : H=SP LAMP ON IN
  These three signals are the input and output signals for switching the audio Dolby circuit ON and OFF. The DOLBY DET IN signal is for detecting the Dolby mode during playback from the audio circuit. The INHIBIT IN signal ignores the playback Dolby detection when the detection results in the Dolby detector is incomplete. The Dolby ON/OFF switch information is supplied to the AV microcomputer through microcomputer M2, and the final Dolby ON/OFF signal is determined by the CH-1/CH-2 DOLBY ON OUT signal at pins 24 and 58.

TAPE	SP		$\overline{SP}$
DOLBY SW	ON	OFF	—
DOLBY MODE	ON	OFF	OFF

Table 5-7. Dolby REC Mode

H : SP MODE	SP			$\overline{SP}$
DOLBY SW	—			—
L : DOLBY DET	L		H	—
L : INHIBIT	H	L	—	—
DOLBY MODE	ON	HOLD	OFF	OFF

Table 5-8. Dolby PB Mode

- P1 (IC401 pin 59) : L=DOLBY LAMP
  This pin is set low when the audio circuit is in the Dolby mode, and the LED on the front panel lights.
- R4 (IC401 pin 5) : H=VIDEO CH-A RE MUTE OUT
- R5 (IC401 pin 6) : H=VIDEO CH-B RE MUTE OUT
  These signals switch ON and OFF the current for the rotary erase heads.
- R6 (IC401 pin 7) : L=VIDEO CH-A REC OUT
- R7 (IC401 pin 8) : L=VIDEO CH-B REC OUT
  These control whether the recording current is to flow to the video heads.
- (IC401 pins 28 to 33, 2) :
  These signals are the communication lines between the AV microcomputer and M2 microcomputer. For further details, refer to section 5-5-4.
- K1 (IC401 pin 18) : 1/2 VD
  The 1/2VD signal is a clock signal which determines the reference timing of the AV microcomputer operation.
- E0 (IC401 pin 34) : L=DOLBY DET
  The signal from the Dolby mode detection circuit during playback on the audio board is supplied to this pin.
- (IC401 pin 35) : L=INHIBIT IN
  This is set to low level when the reliability of the results of the above-mentioned Dolby detector is in doubt.
- (IC401 pin 36) : H=SP LAMP ON
  The signal from the SP mode detector on the video circuit is supplied.
- R11 (IC401 pin 12) : L=SP MODE OUT
  This signal selects the SP mode of the video and audio circuits with cassette casing information.
- R13 (IC401 pin 14) : L=CONVENTIONAL MODE
  Normally, this pin is set high. However, by shorting TP402 with the ground, the mode of the video and audio circuit can be forcibly set to the conventional mode.

5-3-2. Audio Timing Control by AV Microcomputer

Fig.5-11 shows the timing of the audio insert editing in the BVU-800. In U-matic VTRs, there is a clearance of about 9.6mm between the audio erase head and recording/playback head. Therefore, when audio erasing and recording are undertaken virtually simultaneously as in Fig.5-11, there will be an overlap in the recording of the audio signal at the edit IN point and nothing will be recorded at the OUT point. This problem is resolved in the BVU-950 by the AV microcomputer. The head clearance of approximately 9.6mm corresponds in terms of time to about 100msec. The BVU-950 therefore starts erasing 100msec prior to the IN point and stops erasing 100msec prior to the OUT point. This enables audio inserts to be edited perfectly because the signals are recorded accurately from the edit IN point to the OUT point. Fig.5-12 is a timing chart of the audio insert operation in the BVU-950. In order to execute proper insert editing, the command which is 5 frames prior to the IN point must input to the AV microcomputer. However, when an editor is used for editing, the commands are sent in the sequence of the M1, M2 and AV microcomputers and the commands from the editor must arrive 6 frames prior to the IN point in consideration of delay.

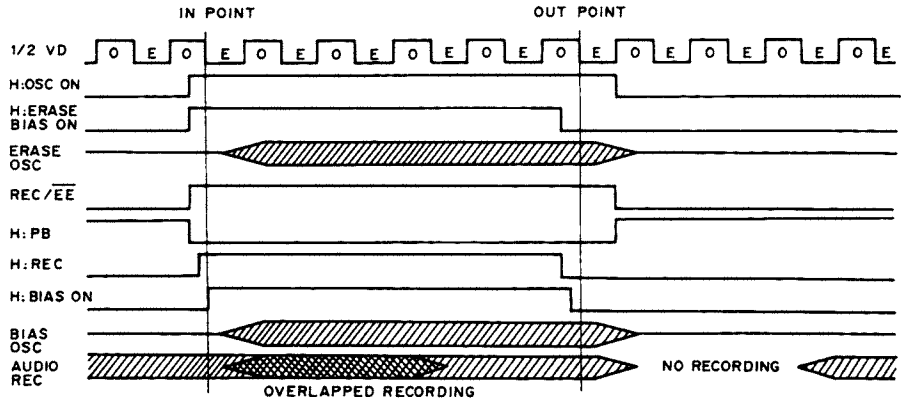


Fig.5-11. Audio Insert on BVU-800

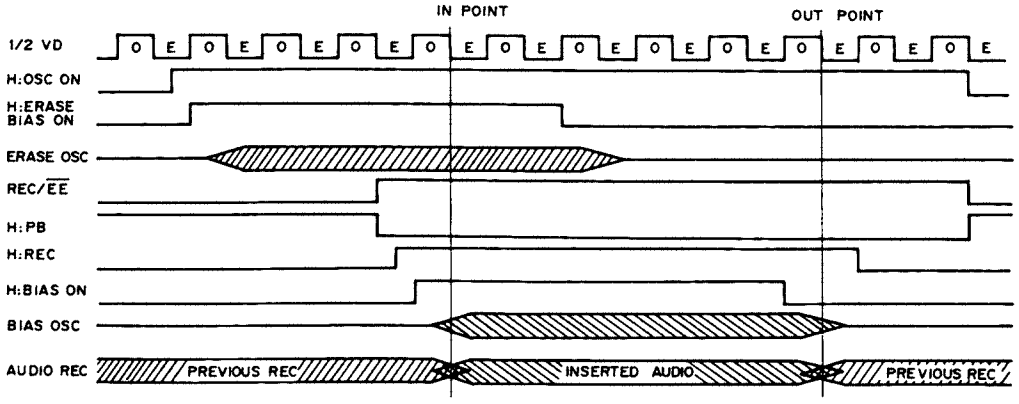


Fig.5-12. Audio Insert on BVU-950

5-4. KY-144 BOARD

5-4-1. KY Microcomputer

The KY microcomputer controls the VTR key panel and it is provided with the following I/O ports :
- Key switches
- LEDs for key switches
- 8-digit 7-segment LED
- JOG/SHUTTLE dial

These I/O data are communicated to the main CPU (microcomputer M1) and controlled.

5-4-2. Digital Hours Meter

When the power is off, the KY microcomputer is set to the standby mode, and the memory contents of the RAM inside the microcomputer is backed up by the battery on the KY board, so that the data is protected.
BT1 on the KY-144 board is the battery that provides backup for the microcomputer power for as long as about 10 years under normal temperature conditions. The KY microcomputer is also backed up by the C8 0.047F capacitor. C8 is provided for setting the KY microcomputer to the standby mode. The supply voltage of the microcomputer is detected at all times at the P3 through P1 port, and when the power is switched off, the microcomputer is set to the standby mode by the software. The operation at this time is performed by the charge voltage of C8.

5-4-3. Key Scanning

PO-4 through PO-7 of the KY microcomputer IC1 output the key scanning pulses for reading the key input information. The respective ports are activated at intervals of 2msec for key scanning, Q1 through Q4 are driven into conduction, and the key information is accepted at port P5 of the KY microcomputer. This means that when one of the PO-4 through PO-7 ports is observed, pulses with a 10msec period will be output.

5-4-4. 7-Segment LED Scanning

Scanning pulses for the 7-segment LED are output from port P6 of the KY microcomputer in order to light the LED for the time display on the front panel. In order to eliminate flicker, one digit is lighted at a scanning pulse period of 128Hz.
The segment data are output from port P4 of the KY microcomputer and a voltage is supplied to the LED by turning Q8 through Q14 to on.

5-4-5. Dial Microcomputer

The DIAL A and B signals, whose phases are shifted by 90° , supplied from the search dial on the front panel as well as the DIAL STILL and high level JOG signals are input to the dial microcomputer (IC7). The dial microcomputer performs the following processing :
- It detects the dial direction using the phase relationship between the DIAL A and B signals.
- It detects the shuttle speed as the 0 through 8 or 0 through −8 data when the VTR is in the shuttle mode.
- It functions as a 4-bit counter in accordance with the rotation speed of the dial when the VTR is in the jog mode.

5-5. COMMUNICATION BETWEEN MICROCOMPUTERS

5-5-1. Software Processing in Microcomputer M1

Fig.5-13 is a software timing of the microcomputer M1. In the microcomputer M1, the software is processed by time-sharing as referenced to the 1/2 VD signal.
In timing 0 through 3 in Fig.5-13, communication between the M1 and M2 microcomputers, communication between the M1 and KY microcomputers, 9-pin connector remote communication, time code reading and CTL signal processing are performed. In timing 4 through 7, time code generator setting, display control, editing control and IN/OUT point control are performed.

5-5-2. Software Processing of Microcomputer M2

Fig.5-13 is a software timing of the microcomputer M2. This microcomputer provides signal processing using the 1/2VD signal and 2VD signal as the reference timing.
In portion 0 in Fig.5-13, the microcomputer M2 communicates with the microcomputer M1. In portion 1, it communicates with the AV microcomputer, and in portion 3, it communicates with the SV microcomputer. In each period, the mechanism information supplied to the microcomputer M2 is processed and such operations as threading and unthreading are processed.

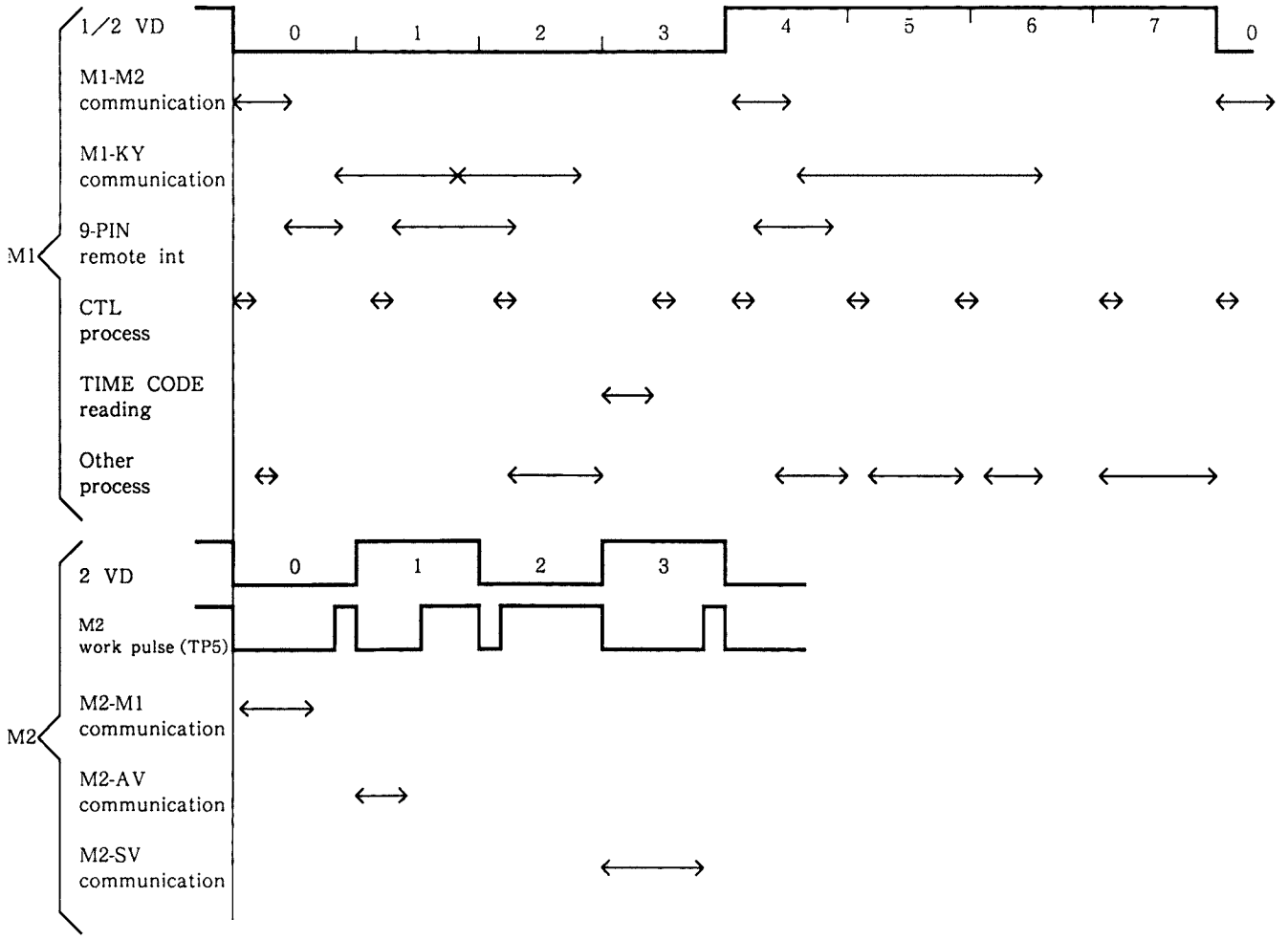


Fig.5-13. M1 and M2 Software Timing

5-5-3. Communication Between Main CPU (M1) and Microcomputer M2

The PA0 through 7 ports of IC1 are used to communicate between microcomputers M1 and M2 with the 8-bit parallel data. The control lines for this communication include the STROBE 0, DATA IN/OUT and STROBE 1 signals. The functions of these signals are described below.

- STB 0 :
  The microcomputer M1 sets this signal to low after the data has been sending the microcomputer M2. And the M1 microcomputer reads the data sent from microcomputer M2 by STB 0 signal.
- STB 1 :
  The microcomputer M2 sets this signal to low after it has been sending the data. And the microcomputer M2 reads the data sent from microcomputer M1 by STB 1 signal.
- DATA IN/OUT :
  This signal specifies the communication direction between these two microcomputers.
- DATA BUS :
  8-bit bidirectional data bus line

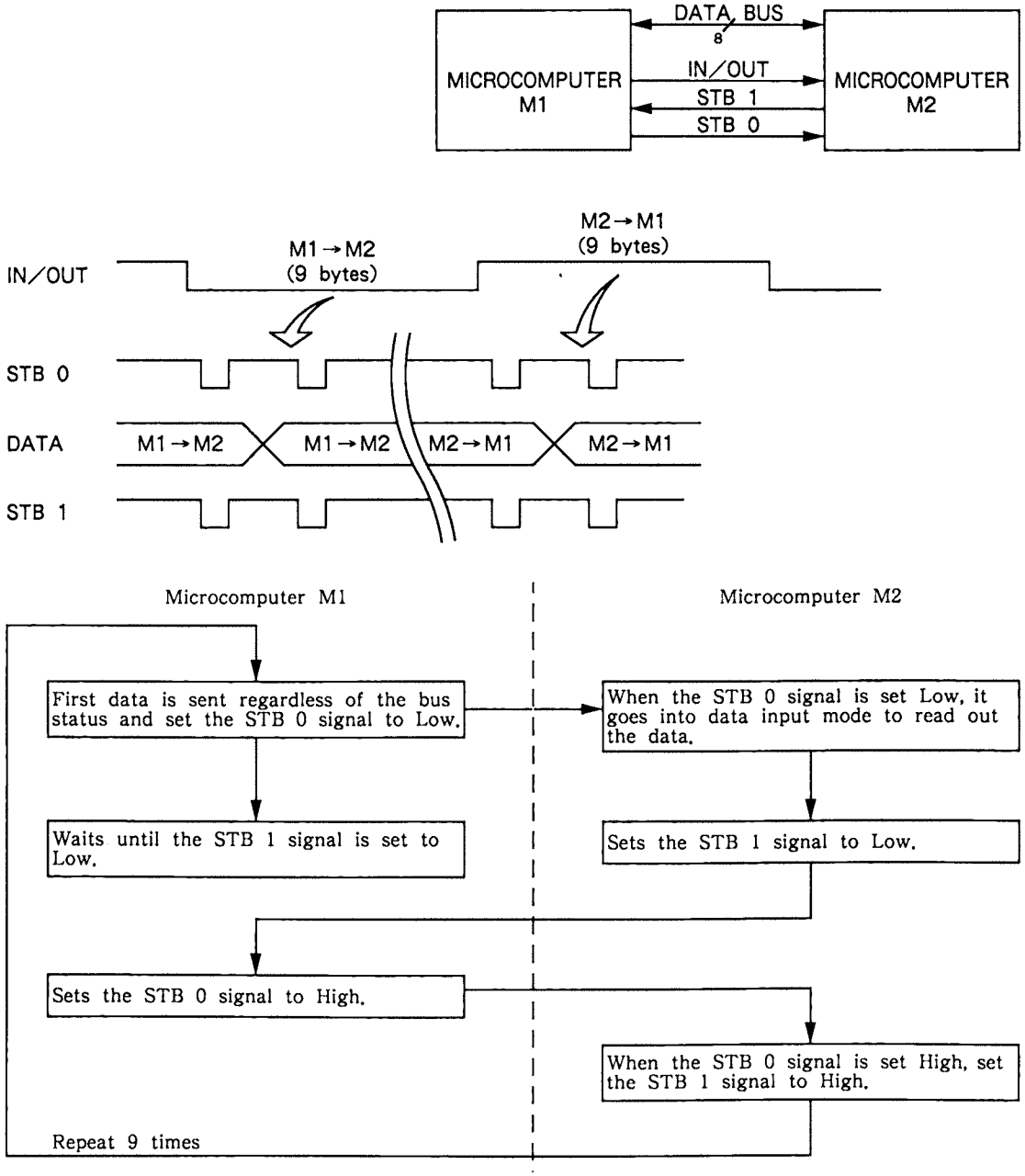

DATA BUS
8
MICROCOMPUTER M1
IN/OUT
STB 1
STB 0
MICROCOMPUTER M2
M1→M2 (9 bytes)
M2→M1 (9 bytes)
IN/OUT
STB 0
DATA
M1→M2
M1→M2
M2→M1
M2→M1
STB 1
Microcomputer M1
Microcomputer M2
First data is sent regardless of the bus status and set the STB 0 signal to Low.
When the STB 0 signal is set Low, it goes into data input mode to read out the data.
Waits until the STB 1 signal is set to Low.
Sets the STB 1 signal to Low.
Sets the STB 0 signal to High.
When the STB 0 signal is set High, set the STB 1 signal to High.
Repeat 9 times

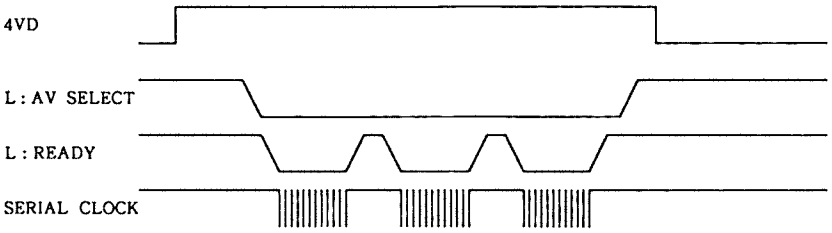
Fig.5-14. M1/M2 Communication

5-5-4. Communication Between M2 and SV/AV Microcomputers

Communication between the SV and AV microcomputers is performed using ports E24 through E26 and R12 through R15 of microcomputer M2.

- SI (serial input) :
  Serial data input from the SV or AV microcomputer to microcomputer M2.
- SO (serial output) :
  Serial data output from microcomputer M2 to the SV or AV microcomputer.
- SC/TO (serial clock) :
  Clock signal for serial data
- CS SV (chip select SV) :
  Low level during communication with SV microcomputer.
- CS AV (chip select AV) :
  Low level during communication with AV microcomputer.
- RDY (ready) :
  Low level when SV or AV microcomputer is ready to start communication.

Fig.5-15 shows the communication between the M2 and AV microcomputers. The M2 microcomputer has a prior claim when it comes to communication between the M2 and AV microcomputers. Communication is started when CS AV of microcomputer M2 is set to low level.
The SV microcomputer is also provided with the initiative after outputting CS SV to low level by M2 when it comes to communication between the M2 and SV microcomputers. The serial clock signal is sent along with the data from the SV microcomputer, and communication is initiated.



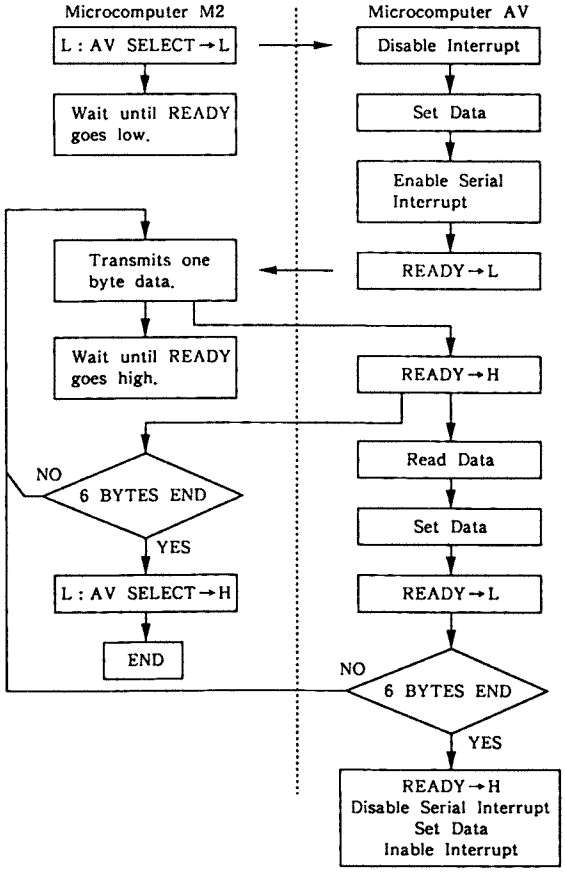


Fig.5-15. M2/AV Communication

5-5-5. Communication Between M1 and KY Microcomputers

Communication between the M1 and KY microcomputers is performed through the SIO on the SY-102 board with the microcomputer M1 acting as the master.

COMMUNICATION PROTOCOL
- Baud rate : 19200bps
- 8-bit data
- Odd parity
- 1 start bit
- 1 stop bit

Fig.5-16 shows the communication between the M1 and KY microcomputers. Communication is synchronized with the 1/2 VD signal. After the time has elapsed from the reference trailing edge of the 1/2 VD signal, 9 bytes data are transferred from microcomputer M1 to microcomputer KY.
Once the KY microcomputer receives normal data from M1, it transfers 7 bytes data to the microcomputer M1. If the data are not received due to a parity error or time error, the KY microcomputer clears the receiving routine and receives the next command.

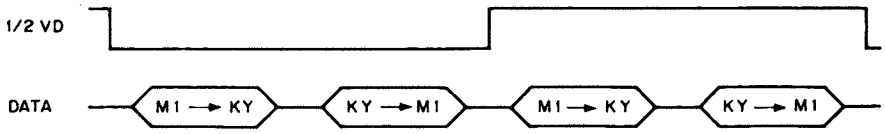


Fig.5-16. M1/KY Communication

5-6. DEFECT ANALISIS IN MICROCOMPUTERS

5-6-1. KY Microcomputer

USE ON TP6 SW BRD. — TO GRND.

• Hardware Check Mode

By shorting TP4 on the KY-144 board with ground, the KY microcomputer enters the hardware check mode in which the following operations are performed. This mode makes it possible to confirm that all the data sent from the KY microcomputer to the 7-segment LED are correct.

While the KY microcomputer is operating, the hardware check mode is entered when PO-1 (TP4) is set to low level.

(1) "8" is displayed on the 7-segment LED for 2 seconds.

(2) "8" is displayed at the least significant bit of the 7-segment LED, and at 0.5 second intervals, the light digit moves up in sequence. This operation is repeated twice for the 8 digits.

(3) All digits from "0" to "F" for the 7-segment LED light at 1 second intervals.

(4) All 35 key lamps light for 4 seconds.

(5) Upon completion of steps (1) through (4), switch check is performed. While switch is depressed, the switch matrix number is displayed on the 7-segment LED. When a multiple number of switches are depressed at the same time, display priority is given to the lowest matrix number. When a switch is not pressed, "– – : – – : – – : – –" appears.

(6) During PO-1 is low, the status in step (5) is maintained, when it is high, the normal operation mode is entered.

```
(1)   88:88:88:88        2sec
                ↓
(2)      :  :  : 8       0.5sec
         :  :  :8        0.5sec
         :  : 8:         0.5sec
         :  :8 :         0.5sec
         : 8:  :         0.5sec
         :8 :  :         0.5sec
        8:  :  :         0.5sec
        8 :  :  :        0.5sec
         :  :  : 8       0.5sec
         :  :  :8        0.5sec
         :  : 8:         0.5sec
         :  :8 :         0.5sec
         : 8:  :         0.5sec
         :8 :  :         0.5sec
        8:  :  :         0.5sec
        8 :  :  :        0.5sec
                ↓
(3)   00:00:00:00        1sec
      11:11:11:11        1sec
      22:22:22:22        1sec
      33:33:33:33        1sec
            :
            :
      EE:EE:EE:EE        1sec
      FF:FF:FF:FF        1sec
                ↓
(4) All key LEDs    Light up for 4sec.
                ↓
(5)   --:--:--:--   KEY SW CHECK MODE
```

Fig.5-17. Display

KEY SWITCH MATRIX

L / H	7	6	5	4	3	2	1	0
1	AUDIO CH-1	VIDEO	ASSEMBLE	PREVIEW	AUTO EDIT	REVIEW	IN	OUT
2	REW	EJECT	SEARCH	EDIT	REC	PREROLL	STANDBY	AUDIO CH-2
3	RECORDER	PLAYER			PB	STOP	F.FWD	PLAY
4				TC	DATA	TRIM (+)	TRIM (–)	ENTRY

LED DISPLAY

		5	–	* (H)	* (L)		

Table 5-9. Key Switch Matrix

• Interrupt Routine Operation Check
The operation of the KY microcomputer itself is normal when pulses with the same period as the key scanning routine are output.

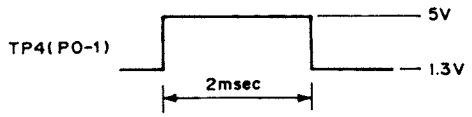


Fig.5-18. Key Scanning Routine Pulse

• Ports PO-3 to PO-7 (IC1 pins 53 to 49)
Key scanning pulses are output every 2msec from these ports. The pulses have a period of 10msec at one port.

• Port P4 (IC1 pins 10 to 17)
The scanning pulses for the 7-segment LED are output at approximately every 1msec interval. The pulses have a period of 7.8msec at one port.

• KY Microcomputer Standby Mode Check
When the power switch is turned off, the supply voltage at pin 1 of the KY microcomputer drops to approximately 4.5V and approximately 0.1sec. later, the KY microcomputer enters the standby mode and the voltage rises. If this voltage appears to drop even further, it means that the KY microcomputer does not enter the standby mode properly.

• Communication Check Between KY and M1 Microcomputers
In synchronization with the 1/2 VD signal, it should be possible to observe the 7-byte data from the microcomputer KY at TP1 (pin 20/IC1) and the 9-byte data from the microcomputer M1 at TP2 (pin 21/IC1). This makes it possible to check that the KY and M1 microcomputers are communicating properly.

5-6-2. Microcomputer M2

• Communication Check
When communication is being performed properly by the microcomputer M2, a high level signal is output at TP8 (pin 29/IC7), when M2 is abnormal condition, a low level signal is output.
• TP5
A pulse which show conditions for communication processing among each block and for interruption processing are output at TP5. When microcomputer M2 works normally, pulse is output at TP5 as shown in Fig.5-19.

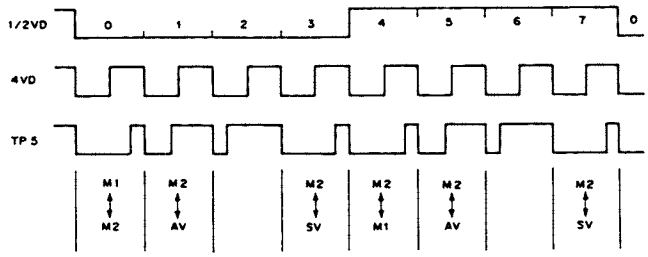


Fig.5-19. Communication Among Microcomputer

5-6-3. AV Microcomputer

The clock signal, 1/2 VD signal and serial signal from the microcomputer M2 are required in order to operate the AV microcomputer properly. These signals should be checked first.
• Communication Check Between AV and M2 Microcomputers
TP401/BC-11
High level : Communication OK
Low leve : Communication between AV and M2 microcomputer NG
• TP403
Because of the software configuration of the AV microcomputer, one pulse is output to the main loop. If the VTR is in the steady state, a pulse with a 1msec period is output. If the VTR is in edit mode, a pulse with a period of approximately 2.5msec is output. This makes it possible for the AV microcomputer software to be processed properly.

5-7. TIMING CHART

Fig.5-20 shows the mode transition of mechanism in the BVU-950.
As shown in the figure, the stable condition of mechanism is indicated as circled modes. The mode transition indicating as arrow portions, are controlled by the system control.

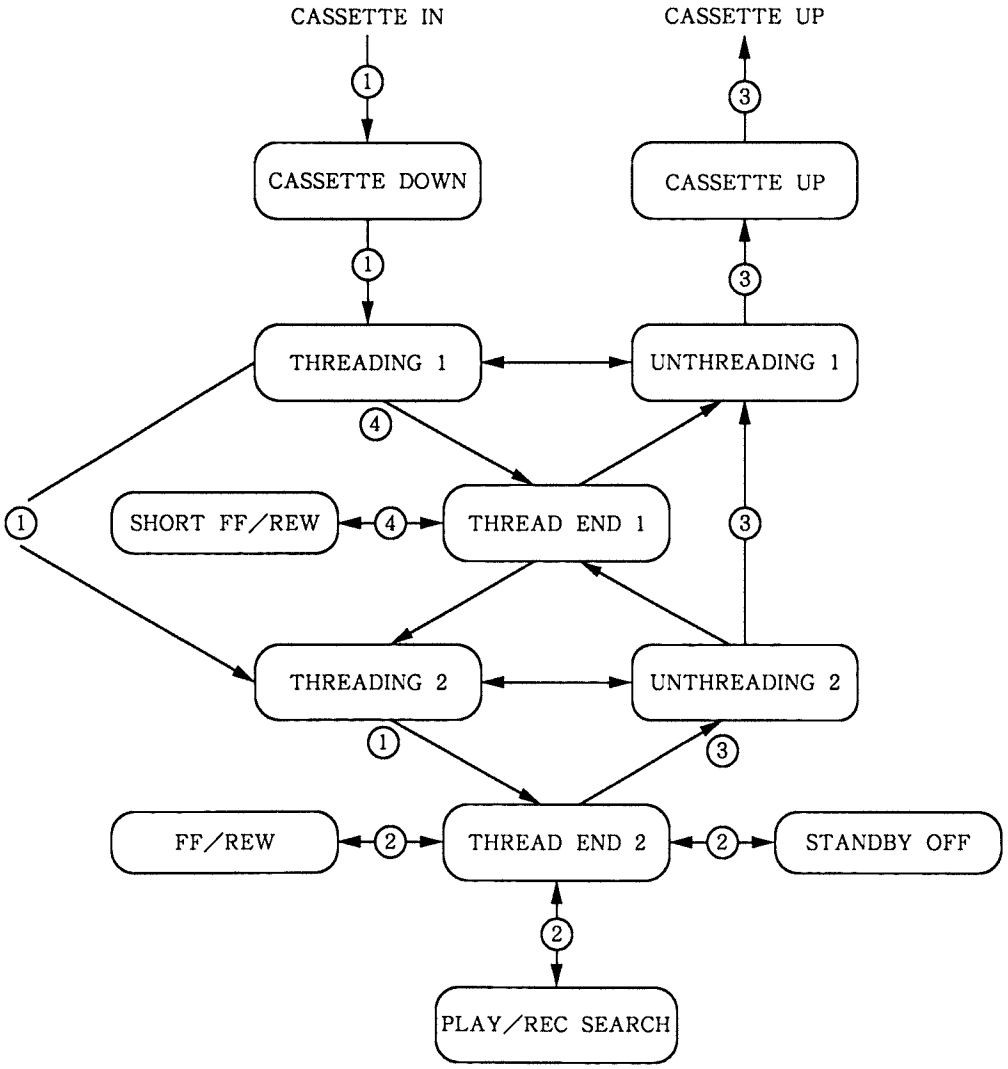


Fig.5-20. Mode Transition of Mechanism

5-8. DIAL MENU OPERATION

The BVU-950 provides dial menu which sets the time code data, superimposed character data and system set-up data.
Fig.5-21 shows the operation of the dial menu.

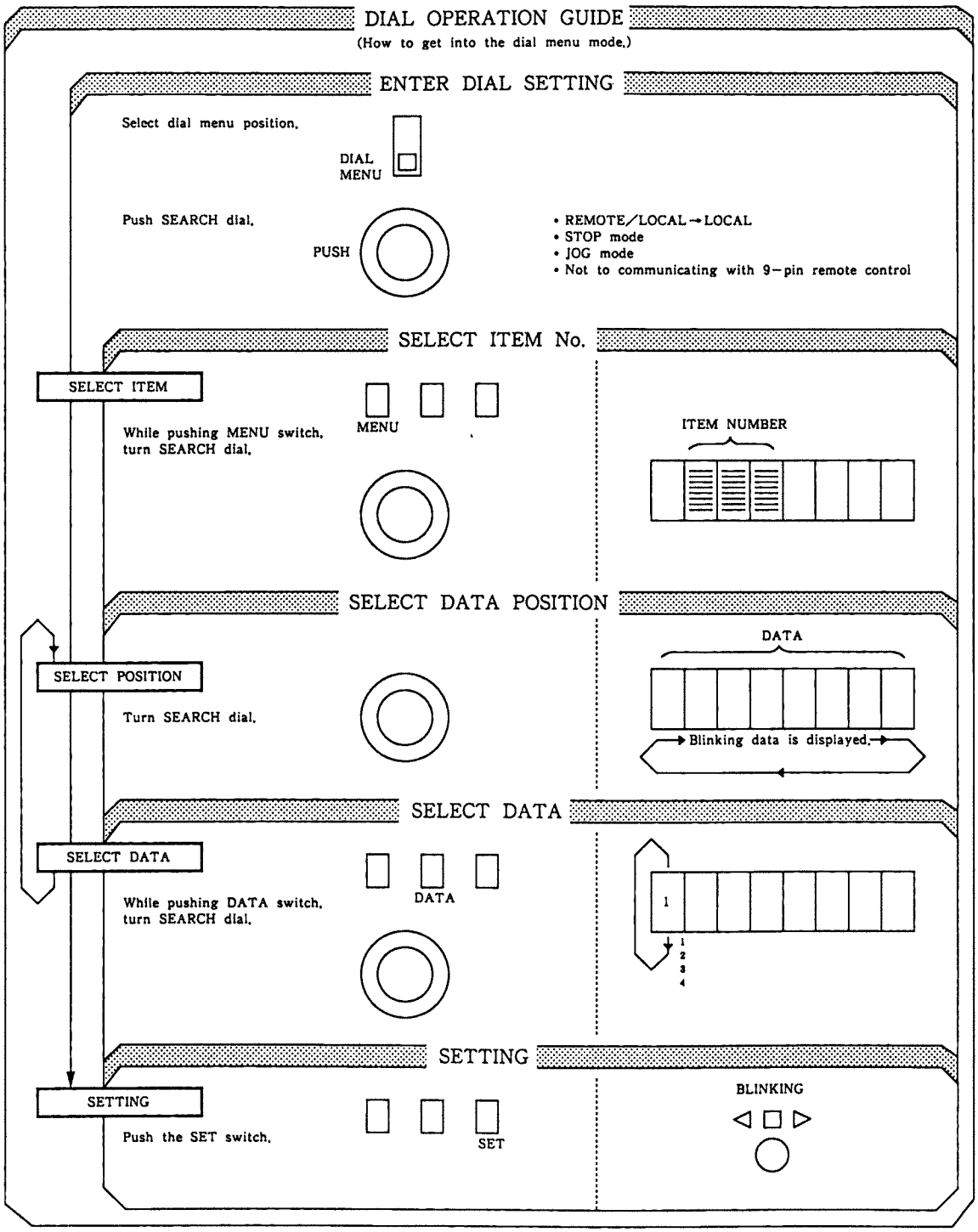


Fig.5-21. Dial Operation Guide

The following menu can be selected by the switches and the JOG dial on the front panel. The menu is consisted of three functions, basic, enhanced and factory/service, however, only basic and enhanced functions can be selected.

BASIC FUNCTION (for daily operation)	101 • TIME CODE SETTING (I) (time code/user bit preset) 104 • TITLE SETTING
⇩	
ENHANCED FUNCTION (for system set-up or maintenance)	201 • ERROR DISPLAY • TIME CODE SETTING (II) (DF/NDF select) • DIGITAL HOURS METER • ANTI-CLOG OPERATION • SYSTEM PRESET 218 • EDITING PRESET

Table 5-10. Dial Menu Operation

BASIC FUNCTION

GROUP	ITEM	FUNCTION		SET & DISPLAY		STANDARD SETTING
				SET	DISPLAY	
TIME CODE SETTING	101 TIME CODE PRESET	TIME CODE SETTING (This value is memorized in NON-VOL RAM.)		O	O	00000000
	102 USER BIT PRESET	TIME CODE SETTING (This value is memorized in NON-VOL RAM.)		O	O	00000000
TITLE RECORDING	103 TITLE (SMALL)	SMALL SIZE CHARACTERS 20×3 ROW	• TC and title can be recorded. • Characters (TIME CODE, TITLE) are selected by commands on the monitor and they are memorized in NON-VOL RAM.	O	O	OFF
	104 TITLE (LARGE)	LARGE SIZE CHARACTERS 20×1 ROW		O	O	OFF
SETUP LEVEL	200 SETUP LEVEL	This is the item to enhance the function. Select "ENHANCE" to move on to the enhance function.		O	O	BASIC

Table 5-11. Basic Function

101 TIME CODE PRESET
This sets the time for the time code which is recorded on the tape in the recorder.

102 USER'S BIT PRESET
This sets the user's bit data which is recorded on the tape in the recorder.

103 TITLE (SMALL)
104 TITLE (LARGE)
These set the characters of the program title, for instance, which is recorded on the tape in the recorder. There are two sizes of characters but only one size can be recorded.

200 SET UP LEVEL
This item shifts the dial menu mode from basic to enhanced. When the enhanced mode is selected, it is possible to set the following enhanced functions.

5-9. ENHANCED FUNCTIONS

ENHANCED FUNCTION

GROUP	ITEM	FUNCTION	SET & DISPLAY		CONTENTS	STANDARD SETTING
			SET	DISPLAY		
ERROR DISPLAY	201 ERROR STATUS	SELF-DIAGNOSTICS (Display Trouble Block)	×	O		——
TIME CODE SETTING	202 DF/NDF SELECT	DROP/NON-DROP FRAME MODE SELECT (EIA Only)	O	O	NDF DF	NDF
	203 PHASE CORRECTION	SMPTE SPECIFICATION (Bit No.27 is set "0" or "1".)	O	O	OFF ON	ON
	204 USER BIT BINARY GROUP FLAG	SMPTE SPECIFICATION (Bit No.43 or 59 are set "0" or "1".)	O	O	Not specified ISO character Unassigned 1 Unassigned 2	NOT SPECIFIED
DIGITAL HOURS METER	205 HOURS METER (DRUM)	DRUM LIFE USE : 0 to 15000H (Incremented by 1H)	×	O		
	206 HOURS METER	OPERATION TIME : 0 to 15000H (Incremented by 1H)	×	O		
ANTI-CLOG OPERATION	207 STILL TIMER	TIMER SELECTION IN STILL MODE (0.5, 1.5, 10 to 50sec/1 to 8min)	O	O	0.5, 1.5, 10, 20, 30, 40, 50sec 1 to 8min	8min
	208 TAPE PROTECTION MODE	Protection mode select when still time is over.	O	O	STEP FWD, STANDBY OFF	STEP FWD
SYSTEM PRESET	209 SELECTION FOR SEARCH DIAL ENABLE	Select the way to enter search mode, by pushing SHUTTLE button or SEARCH dial.	O	O	DIAL DIRECT VIA SEARCH BUTTON	DIAL DIRECT
	210 DRUM ROTATION IN STANDBY OFF	SELECT DRUM ON/OFF IN STANDBY OFF MODE	O	O	OFF ON	OFF
	211 TAPE TIMER DISPLAY	CTL DISPLAY MODE : ±12H or 24H	O	O	*±12H, 24H	±12H
	212 AUTO EE SELECT	During PB/PB • EE switch is set to PB • EE, VTR goes into EE mode in FF/REW/STOP or STOP only.	O	O	STOP/FF/REW STOP	STOP/FF/REW
	213 MONITORING SELECTION FOR VTR TO VTR EDIT	Enables to watch player's picture on a recorder's monitor.	O	O	AUTO SWITCH RECORDER ONLY	RECORDER ONLY
	214 PREROLL TIME	Preroll time can be selected.	O	O	0 to 15sec	5sec
EDITING	215 AUTOMATIC PREROLL ENTRY	Select whether the time is entered as an in-point or not when the preroll key is pressed.	O	O	DISABLE ENABLE	ENABLE
	216 SYNCHRONIZE	Synchronization ON/OFF selection when the preroll time is less than 5sec.	O	O	OFF ON	OFF
	217 EDIT DELAY	Adjust command timing which is sent from editor for proper editing.	O	O	2 FRAMES 6 FRAMES	6 FRAMES
	218 PINCH ON DELAY	Adjust pinch-on delay time.	O	O	0, 1, 2,.... 14, 15,	9
	219 LOCAL FUNCTION ENABLE	Select the acknowledgement of local keys during remote mode.	O	O	STOP & EJECT ALL ENABLE ALL DISABLE	STOP & EJECT
	220 FREEZE MODE	Contents of FREEZE mode can be selected.	O	O	STBY OFF FREEZE IN AUTO FREEZE	SW1=OFF SW2=OFF
	221 CHARACTER REC ENABLE	Select wheter superimposed character is to be record on tape or not.	O	O	ENABLE DISABLE	ENABLE

Table 5-12. Enhanced Function

201 ERROR STATUS

This indicates the cause in the VTR applying when AUTO OFF is detected.

- Error 01 REEL STOP
- Error 02 SLACK
- Error 03 CAPSTAN ERROR
- Error 04 DRUM STOP
- Error 05 REEL ERROR
- Error 10 DEW
- Error 20 SYSTEM ERROR
- Error 30 LED OFF

202 DF/NDF SELECTION

This selects whether the time code which is recorded on the tape in the recorder is to be set to the drop frame mode or non-drop frame mode.

203 PHASE CORRECTION

The time code signal is coded by the bi-phase mark system, and it is not definite as to whether bit 0 will start at the rising or falling edge.

However, by setting bit 27 to "1," a start can always be made at the falling edge. This process is known as phase correction and this item serves to switch it ON and OFF.

204 USER'S BIT BINARY GROUP FLAG

The condition being used for user's bit is defined by this item.

205 HOURS METER (DRUM)
This meter is for ascertaining the operating time of the drum. It counts under thread end and drum ON conditions as well as in any mode except standby off. The display indicates the count in 1-hour units.

206 HOURS METER (TOTAL)
This meter is for ascertaining the total operating time of the VTR. It counts at all times when the power is on.

207 STILL TIMER
When the still mode is established for a prolonged period of time, the VTR is automatically entered into the tape protection mode in order to prevent head clogging and tape damage. This item serves to set the time, and when the still mode continues for the amount of time which has been set, the operation set by item No. 208 will result.

208 TAPE PROTECTION MODE AFTER STILL MODE
After the still timer in item No. 207 has been activated, the VTR enters to protect the tape. Item No. 208 selects this mode. This establishes the standby OFF mode, stops the drum, reduces the tape tension and advances the tape in the forward direction at 1/30th of the normal tape speed.

209 SEARCH MODE ENTRY
Under normal conditions, the VTR will automatically enter the search mode when the search dial is pressed or rotated. However, in order to safeguard against malfunctioning, it can be prevented from entering this mode if the SHUTTLE/JOG button is not pressed.

210 DRUM ROTATION IN STB OFF
Under normal conditions, the VTR stops the drum motor and reduces the tape tension in the standby OFF mode.
In order to reduce the amount of time when transferring the VTR from the standby OFF mode to another mode, this item allows only the tape tension to be reduced and the drum motor to be kept rotating in the standby OFF mode.

211 CTL DISPLAY SELECTION
This selects whether the time display on the front panel is to be set to the 24-hour mode or ±12-hour mode for indication based on the CTL signal.

212 EE MODE SELECTION
The VTR will automatically set to the EE mode in the stop, fast forward and rewind modes when the PB/PB·EE switch on the front panel has been set to the PB·EE position.
This item can be set so that the EE mode is established only during the stop mode.

213 ONE MONITOR MODE
When the editing is performed with one player and one recorder, this item enables the playback pictures from the player to be monitored on a monitor at the recorder side. In other words, when the RECORDER switch on the recorder's front panel is pressed, the picture at the recorder side can be monitored and when the PLAYER switch is pressed, the playback picture at the player side can be forcibly monitored.

214 PREROLL TIME
The preroll time which is used for editing can be set in 1-second units from 0 to 15 seconds.

215 IN-POINT ENTRY BY PREROLL BUTTON
Under normal conditions when the PREROLL key is pressed, the point at which the key was pressed is entered as the IN point and this point is prerolled. However, if this item is set as "NO," it is possible for that point not to be entered as the IN point and that after prerolling for only the playback operation to be performed.

216 SYNCHRONIZE
When this item is set to on, and the preroll time has been set to 5 seconds or less, item No. 214 is automatically set to 5 seconds and synchronization is carried out.

217 EDIT DELAY
The audio and video signals can be edited properly by the BVU-950 provided that the REC command is received 6 frames prior to the IN point, when an editor is used for editing.
Under normal conditions, the edit delay of the BVU-950 and editor are set to 6 frames.

2 FRAME	BVE-1000, BVE-3000, IF-500
6 FRAME	BVE-5000, BVE-800, BVE-900

Table 5-13. Edit Delay

218 PINCH ON DELAY
This item can set the time duration from the PLAY command output timing to tape start timing.

219 LOCAL FUNCTION ENABLE

When setting the REMOTE/LOCAL switch on the front panel to REMOTE position and the REMOTE 1/REMOTE 2 switch on the sub-control panel to REMOTE 1 (9P) position, reception of the keys on the front panel can be selected.

However, when controlling the BVU-950 through the 24P connector, this item is prohibited.

- STOP and EJECT keys only are enabled.
- All keys are enabled.
- All keys are disable.

220 FREEZE MODE

Contents of FREEZE mode can be selected according to the SW1 and SW2 setting.

- SW1=ON : STANDBY OFF FREEZE mode
- SW2=ON : IN POINT AUTO FREEZE mode

221 CHARACTER REC ENABLE

This item can be selected whether the superimposed character is to be record on tape or not.

SECTION 6
MECHANICAL DESCRIPTION

6-1. OUTLINE

The mechanical section of this unit is designed based upon the type 7 series's tape transport with improvements to take full advantage of BVU performance. This means that there are less parts than the tape transport of the BVU-800 series and the cost has been reduced.

There are the following three reasons for that the mechanism of the BVU-950 is in common with that of type 7.

1. Because type 5 has a tape transport which already has a performance record of 100,000 units and enjoys practical application.
2. Because it is possible to create an ideal and stable tape transport by improving the superior type 5 mechanism.
3. Because the mechanism of type 7 is one-piece and extremely superior in the areas of cost and high precision.
   As a result, transient tape tension becomes half than the BVU-800 series and the tape transport loss is also improved approximately 20%.

The following explanation deals with each block.

- The electrodeposition finish of the connector panel and bottom panel and the ornamental panel have been abolished.
- The controls and connectors are mounted directly on the board, eliminating harnesses.
- Hinge mechanism for opening and closing the key panel has been changed (Refer to Fig.6-1).
  While a six-stage system was used for opening and closing the key panel in the BVU-800 series, this unit uses a four-stage (90° /60° /30° /0°) system. This system allows the angle of opening/closing to be altered by releasing the lock from the front when the unit is rack mounted.
- The height of this unit has been reduced to five span size, the same as type 5. This allows this unit to be substituted for type 5 models which are already rack mounted, upgrading the system.
- Use of pressure-type connectors
  This allows the connector pins to be brought into contact with the lead wire without removing the coating.
- Elimination of hours meter
  Time is measured by a digital hours meter inside the microcomputer.

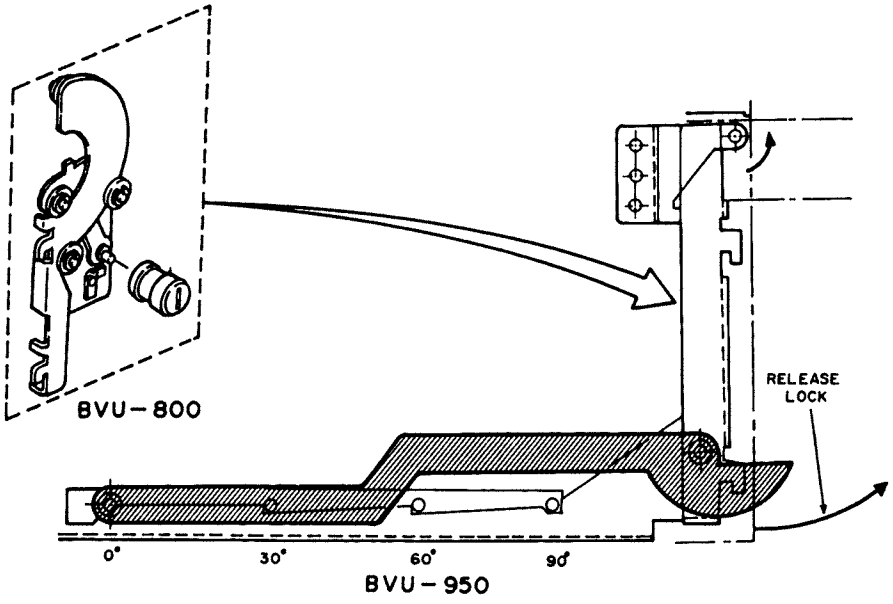


Fig.6-1. Opening and Closing Mechanism

6-2. TAPE TRANSPORT SYSTEM

This unit uses the same tape transport (diecast chassis) as type 7 and type 9 in order to retain the functions and performance of the BVU-800 series. In type 5, the slant base and chassis are separate while in types 7 and 9, they form a single unit. Thus, dimensional precision is improved and a stable tape path can be obtained. Moreover in this unit, the tape is transported in the threaded states in the FF and REW modes. Consequently, there is no mode corresponding to the FR STOP mode of types 5 and 7. In addition, the reel system is directly driven by the tension servo in the same manner BVU-800.

Comparing the BVU-800 and BVU-950, due to differences in the tape loading method of the two, the total tape wrapping angle of the guides, drum, and heads in the BVU-950 is approximately 80° greater. However on the other hand, as the wrapping angle of the fixed guides is 100° less, there is less overall loss in the tape transport system when compared to the BVU-800. This machine uses many roller guides with ball and metal shaft bearings to reduce transport loss. Furthermore, the following points have been improved in the transport system of this unit in comparison to type 5.

1. Leading guide and T (take-up) side drawer guide have been changed to ball bearings.
2. The material for the roller guides has been changed from plastic to metal.
   As an example, the table below shows the tension in the T side reel section when 20g of tension is applied by the reel motor on the S (supply) side.

	FF	REW
BVU-950	104g	126g
BVU-800	117g	157g

Table 6-1

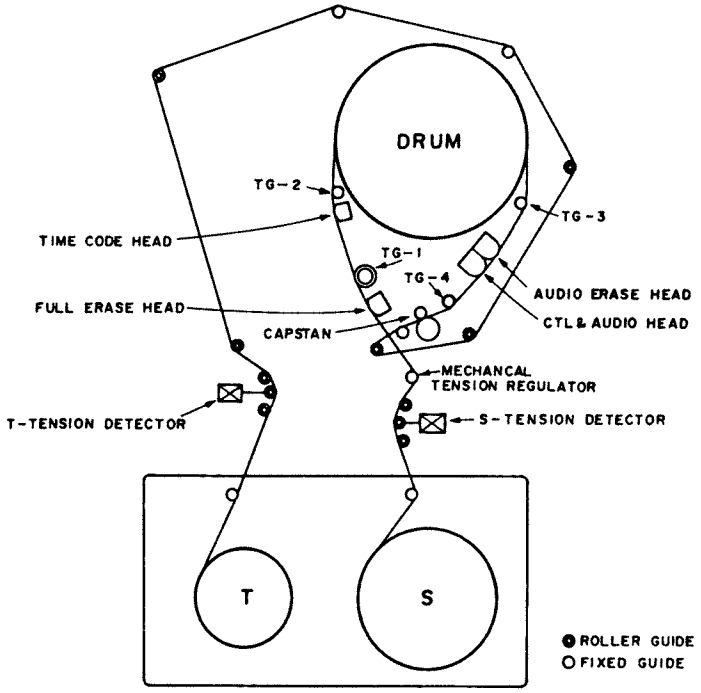


Fig.6-2. BVU-800

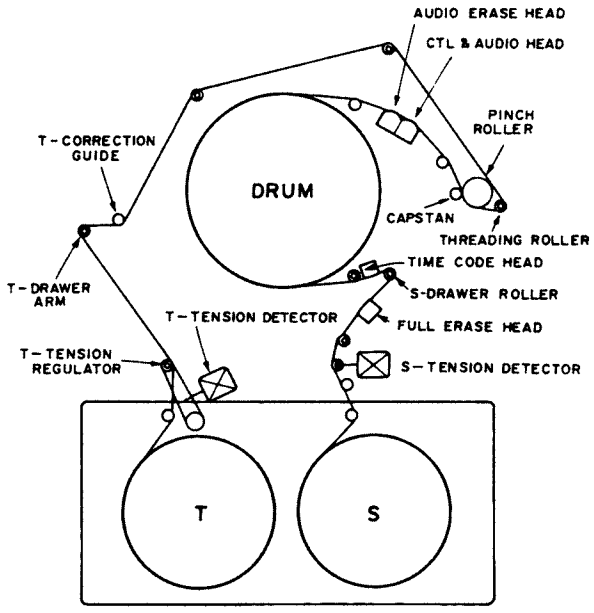


Fig.6-3. BVU-950

6-3. DRUM ASSEMBLY

The drum assembly of this unit is based upon the drum assembly of the VP-5020 with the addition of video, flying erase and impact heads. Necessary revisions have been made to configure a editing unit with the unit converted to SP use of improving the characteristics. Although the same video head as the BVU-850 is used. The motor and rotary transformer sections are the same as the VP-5020, and the same compact slip ring as the BVW-25 is used.

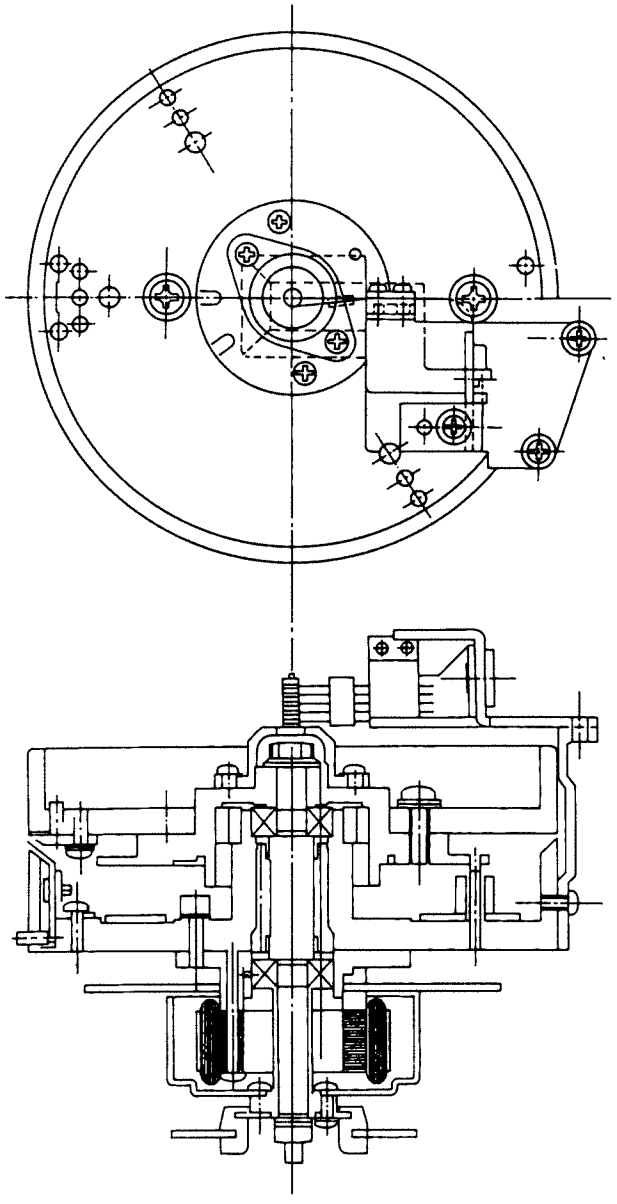
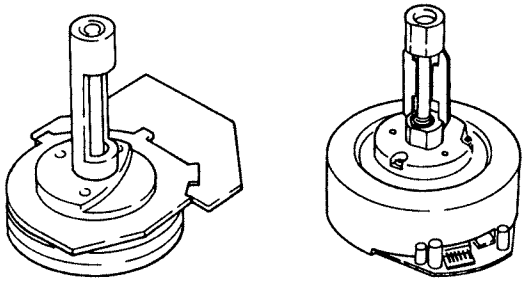


Fig.6-4. Drum Assembly

6-4. CAPSTAN MOTOR

The compact BHF-1900 series motor adopted in the VP-5020 is used for the capstan motor. The capstan shaft is made straight through the use of a V^2 servo. This eliminates the different varieties of capstan motors and simplifies processing. Furthermore, by making the shaft straight, the dimension precision of the shaft is stabilized and wow and flutter characteristics are improved. Wow and flutter has been reduced in this unit to 0.15% versus 0.2% for previous models.



BVU-950 BVU-800 Series

Fig.6-5. Capstan Motor

6-5. REEL MOTOR

The reel motor uses a direct drive system. BVU-800 used a reel motor manufactured by Canon while this machine uses a motor produced by Phillips. This extends the guaranteed operation time of the reel motor from the previous 3000 hours to 4000 hours.

6-6. SOLENOIDS

This unit uses three solenoids: T side brake solenoid, S side brake solenoid and pinch roller solenoid. These are the same open-type solenoids as are used in the type 7 series.

6-7. STATIONARY HEADS

The audio head and full erase head are the same as those of the BVU-850. The audio head is a sendust-type for superior high range characteristics.
As the previous time code head had a large shape, a more compact time code head has been newly adopted in this unit. In the previous time code head for U-matic VTRs, a CTL track section was included in the time code head. In the BVU-950, however, the tape is fast forwarding and rewinding as tape is threaded, the CTL head is included in the time code head.

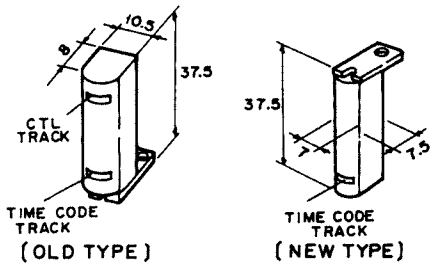


Fig.6-6. Time Code Head

6-8. SENSORS

T and S sides tape tension are detected by the light-emitting diodes and CdS elements, the same as the BVU-800. The construction on the S side is the same as BVU-800 and the construction on the T side is the same as type 5. Rotation detection of the reel is made by the FG ring and DME. The DME element is the same as BVU-800. Detection of tape top and tape end is made a combination of light-emitting diode and phototransistor, the same as the type 7 series. Photocouplers are used for the six sensors listed below.

- Cassette size discrimination
- SP tape detection
- Miss REC detection
- Thread End-1 detection
- Thread End-2 detection
- Unthread End detection

6-9. PINCH ROLLER

The pinch roller of this unit is the same as the type 5 series.

6-10. ILLUMINATION LAMPS

Previously, the most frequent reason for service calls was to replace a blown VTR lamp. This unit uses LED for display in the key panel section, illumination of meters, illumination within cassette compartment, etc., greatly improving reliability.

SECTION 7
TBC

7-1. OUTLINE

The BKU-901/BKU-901A is a digital time base corrector used with the subcarrier low-frequency conversion BVU-950 (NTSC). This unit has a wide correction range of 15Hp-p and stable B/W playback picture can be obtained. Refer to the block diagram in Fig.7-1.
Because the BKU-901 and the BKU-901A have almost identical functions, the BKU-901 only is described.

7-2. CONSTRUCTION

This unit consists of the following circuits.
- Clock generator
- A-D/D-A converter
- Memory
- Sequence control circuit
- Processor
- Secondary beat canceller
- Sync signal generator

The circuitry of the BKU-901 is configured in virtually the same way as that of the BVT-800 although widespread use of ICs throughout the circuits has enabled all the circuitry to be configured on the TBC-5 board.

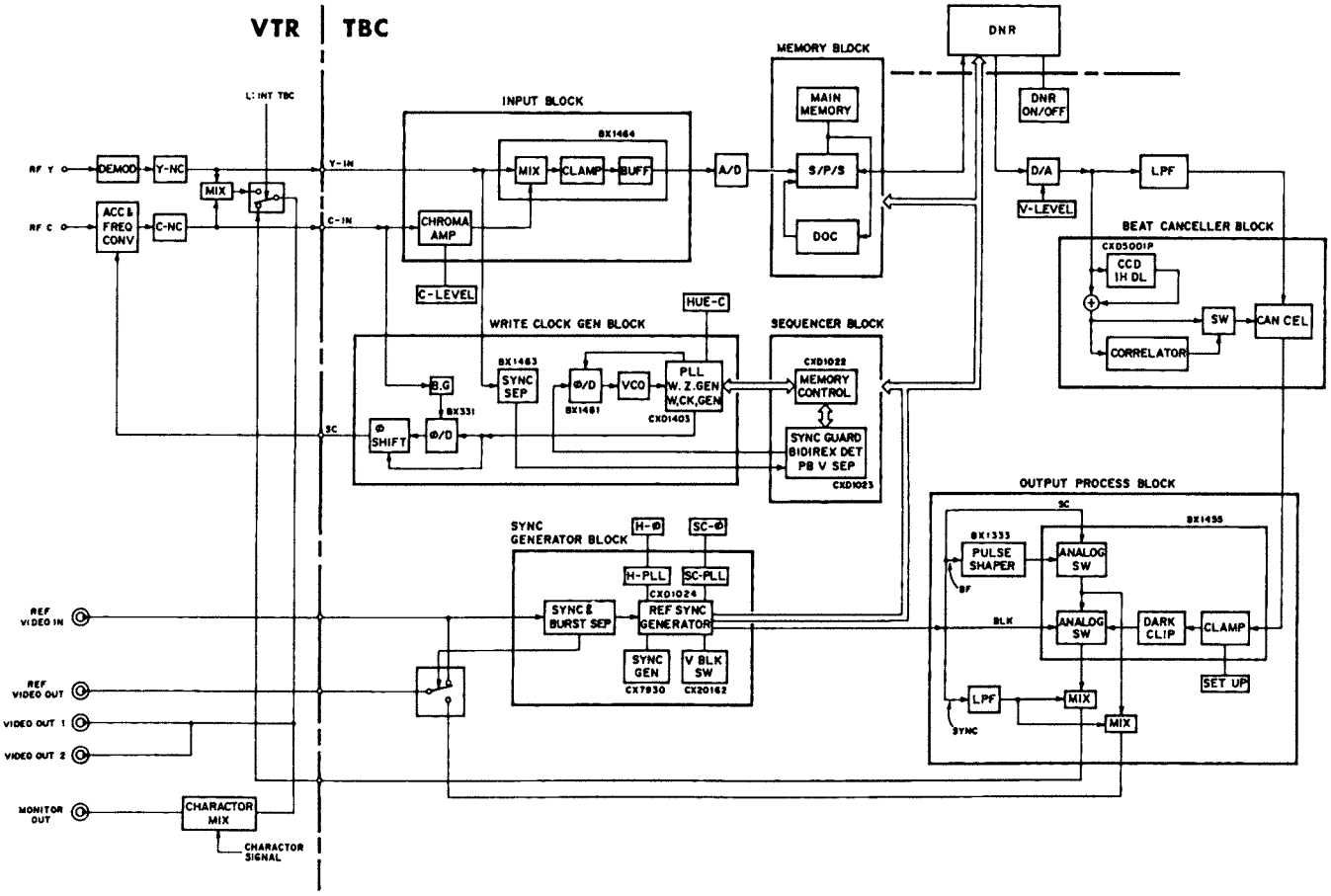


Fig.7-1. TBC Block Diagram

7-3. SIGNAL PROCESSING

The processing of the playback video signal from the video circuit is described below.
The BKU-901 is a plug-in type of time base corrector for the BVU-950, and thus it performs its various processing operations in the direct mode by the return subcarrier.
In this mode, the subcarrier containing a time base error is fed to the video circuit. The same amount of time base error in the Y signal is further added to the chroma signal at the video side, and mixed signal at the TBC board is fed to the A-D converter. The playback video signal input to the A-D converter is sampled using a clock (WRITE clock), generated from the H sync of the playback video signal. This is A-D converted into an 8-bit parallel PCM signal. The sampling frequency is 4fsc.
The digitized video signal is sent to the dropout compensator (DOC). Usually, the video signal by-passes this compensator. However, when a dropout occurs in a VTR, the dropout portion is replaced with a signal that precedes it by 1H period. This dropout compensator is composed of the chroma signal inverter circuit and digital filter which separates the digitized video signals of the line before into the Y and chroma signals.

Next, the 8-bit digital signal is written into the 16-line memory. The written data is then read out by the clock pulse (READ clock) which has been generated from the reference signal that is free from time base errors. It is then sent to the D-A converter and converted into an analog video signal. The secondary beat components are cancelled out by the secondary beat canceller circuit. The signal is then blanked and the burst signal is added. In the final stage, the horizontal sync sigal is added and the composite signal is sent as the output signal.

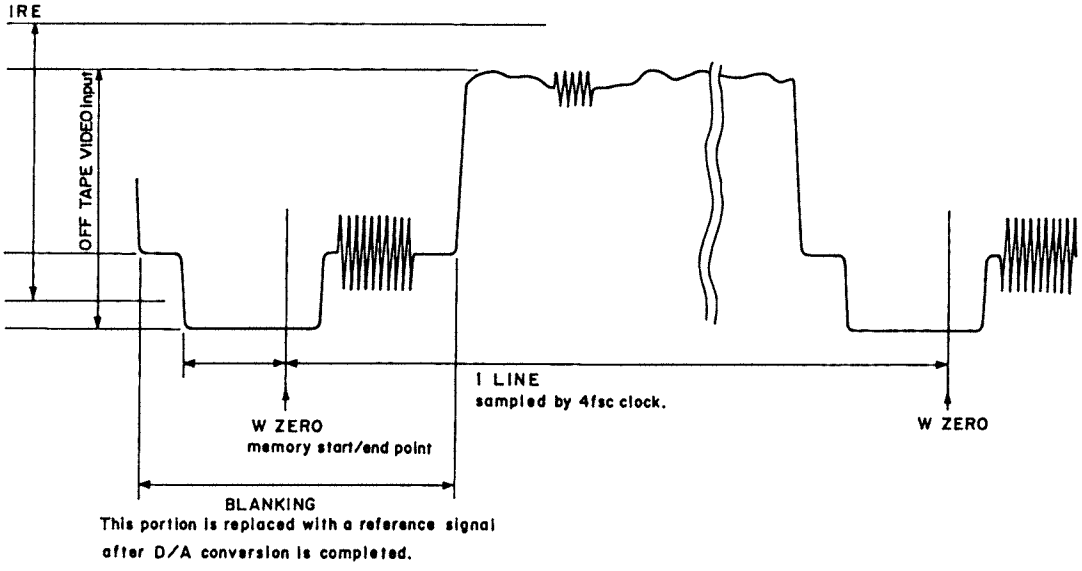


Fig.7-2. Digitalizing the PB Video Signal

7-4. HETERODYNE COLOR CIRCUIT

7-4-1. Outline

To correct the time base in the TBC, the input video signal has to be the same time base error and frequency interleaving relationship between the Y signal and chroma signal.
In the chroma signal low-frequency conversion VTRs, the phase and frequency fluctuations have been corrected and the chroma signal is mixed with the Y signal whose fluctuations are not corrected. This mixed signal is then sent as an output signal. Therefore, there is no frequency interleaving relationship between the chroma and Y signals.
In the BKU-901, signal processing has been previously performed in the return SC mode in order to meet the interleaving relationship between playback Y and chroma signals from the chroma signal low-frequency conversion VTR. Thus the TBC produces the subcarrier from the Y signal and feeds the subcarrier back to the VTR. The VTR performs frequency-conversion using the frequency interleaving subcarrier as a reference signal instead of the internal SC oscillator. As a result, a playback video signal which contains the frequency interleaving relationship between the Y and chroma signals is output from the VTR.

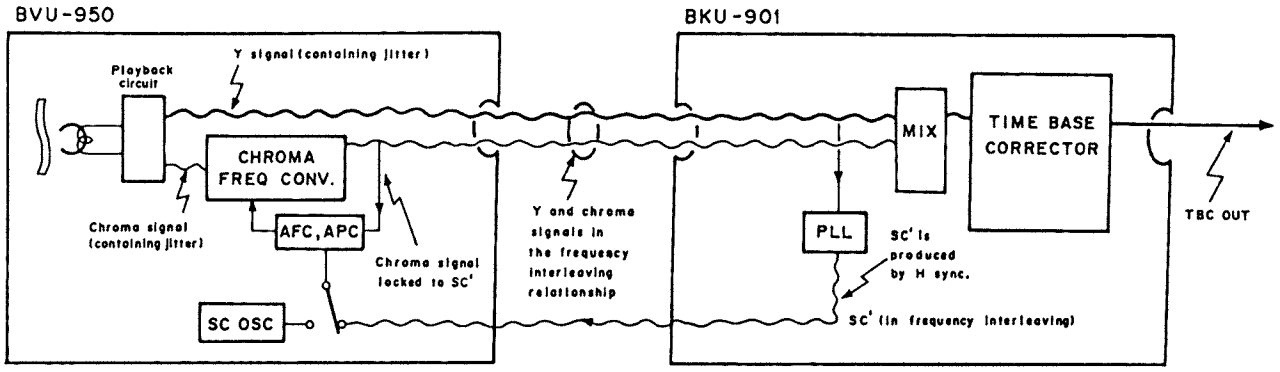


Fig.7-3. Connection of TBC to Low-frequency Conversion Type VTR (Return SC Direct Mode)

7-4-2. Return SC Direct Mode

The demodulated Y signal from the VTR is input to the TBC-5 board in order to separate the horizontal sync signal (H SYNC). Using the SELECT H signal, a pseudo sync due to noise is removed, VCO (4fsc) is oscillated by the selected signal (SELECT H) and divides the frequency into 1/4 to produce a subcarrier (fsc). The 4fsc VCO output is divided into 910 to produce the fH period (count H), and the 4fsc voltage-controlled oscillator (VCO) is controlled by the difference in phase from the SELECT H signal.
The 4fsc VCO is locked to the input fH by this AFC loop.
In this case, fsc is represented as fsc$\pm\Delta$f as shown in Fig.7-4 since it contains a Y signal time base error.
In the return SC DIRECT mode, the subcarrier containing the time base error is used as a RETURN subcarrier.
The phase of the burst signal taken out from the playback chroma signal and the phase of the WRITE SC are then compared and, by controlling the WRITE SC phase with the resulting error, the hue fluctuation which may occur in the search mode is prevented.
The phase-controlled SC is sent to the video circuit as a RETURN subcarrier. In other words, a loop between the video circuit and this circuit is formed so that the PB burst signal phase will coincide with the subcarrier fsc phase generated by the PB sync signal.

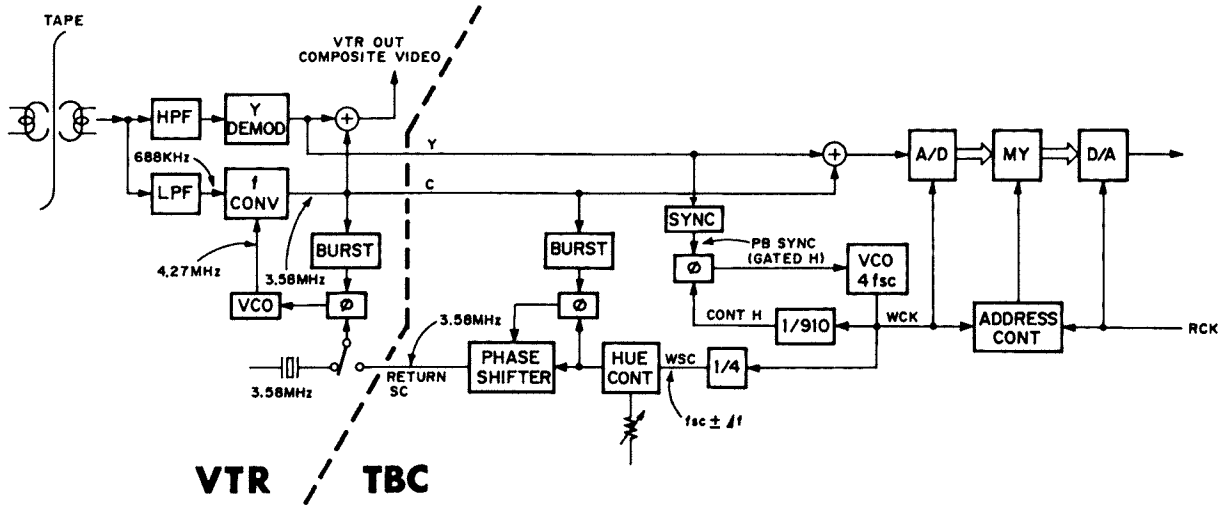


Fig.7-4. Return SC Direct Mode

7-4-3. Return SC Circuit

The WRITE SC signal is output from pin 36 of IC307 on the TBC-5 board, and it enters the HUE control circuit which is composed of IC301 and IC302. The HUE control is perfomed by changing the WRITE SC phase. The WRITE SC phase is changed in accordance with the time constant of monostable multivibrator with the voltage that can be varied by the HUE control on the TBC remote controller. (Namely, when the WRITE SC phase changes, RETURN SC phase also changes so that the phase of the chroma signal including the burst signal changes, too. Consequently, relative phase between the reference burst signal which is replaced in the final stage and the chroma signal is changed so that the HUE of the TBC OUT changes.)
RV301 is designed to adjust the preset value of the HUE control.
The RETURN SC signal then passes through the HUE correction circuit which is composed of IC307 through 312.
The chroma signal sent from the video circuit enters pin 34 of IC307 and is output from pin 33. The burst signal contained in this signal is taken out by IC308; its phase is compared with the phase of the WRITE SC signal in the IC310 phase comparator, and the resulting error signal appears at TP307. This error signal is amplified by IC311 and, by controlling the time constant of the monostable multivibrator IC312, the phase of the WRITE SC signal is controlled, and the signal is sent to the video circuit as the RETURN SC signal.

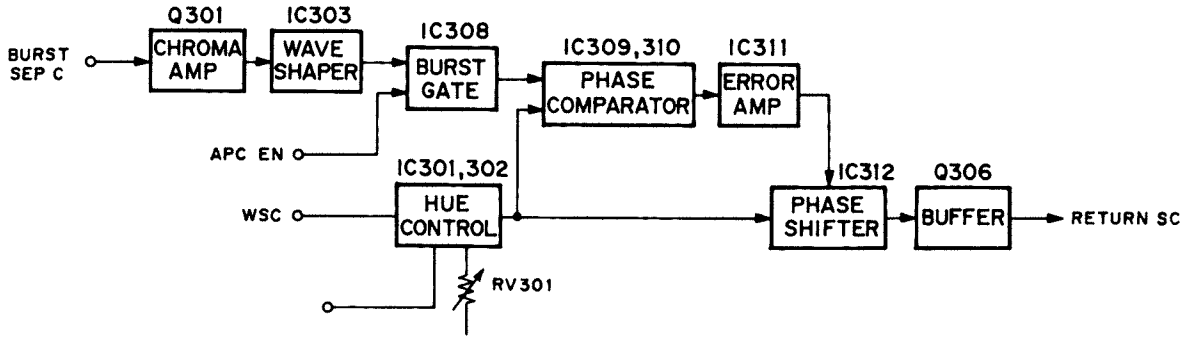


Fig.7-5. Return SC Circuit

7-5. A-D CONVERTER

The playback Y signal, which has sent from the video board, is mixed with the chroma signal, its DC level is clamped by the clamp circuit and the signal is sent to the A-D converter IC104.

7-5-1. Input Circuit

The playback Y signal, which has sent from the video board, is input to IC101 after passing through the buffer Q101. Similarly, playback chroma signal, which has sent from the video board, is input to the chroma amplifier IC105 after passing through the buffer Q104. Gain controlled chroma signal is passed through the switcher consisting of Q105 and Q106 and is input to IC101 where it is mixed with the playback Y signal.
Switcher Q105 and Q106 mute the chroma signal in the B/W mode or in the FF/REW mode.

7-5-2. Clamp Circuit

The A-D converted video signal should have a constant pedestal potential. In this unit, the feedback type clamp circuit is formed with differential amplifier. The feedback loop is formed inside the IC101. Then, the pedestal level is sampled using a pulse produced by the SELECT H (periodic PB H SYNC) signal.
The full-type integration hold circuit in the next stage is controlled using a CLAMP OFF signal which detects the absence of the SELECT H signal. Therefore, if the clamp pulse senses no SELECT H, the preceding level can be held. The difference voltage between the reference voltage produced by RV102 and the video signal pedestal voltage is integrated and amplified inside IC101. Then, the error voltage is fed back to the differential amplifier.

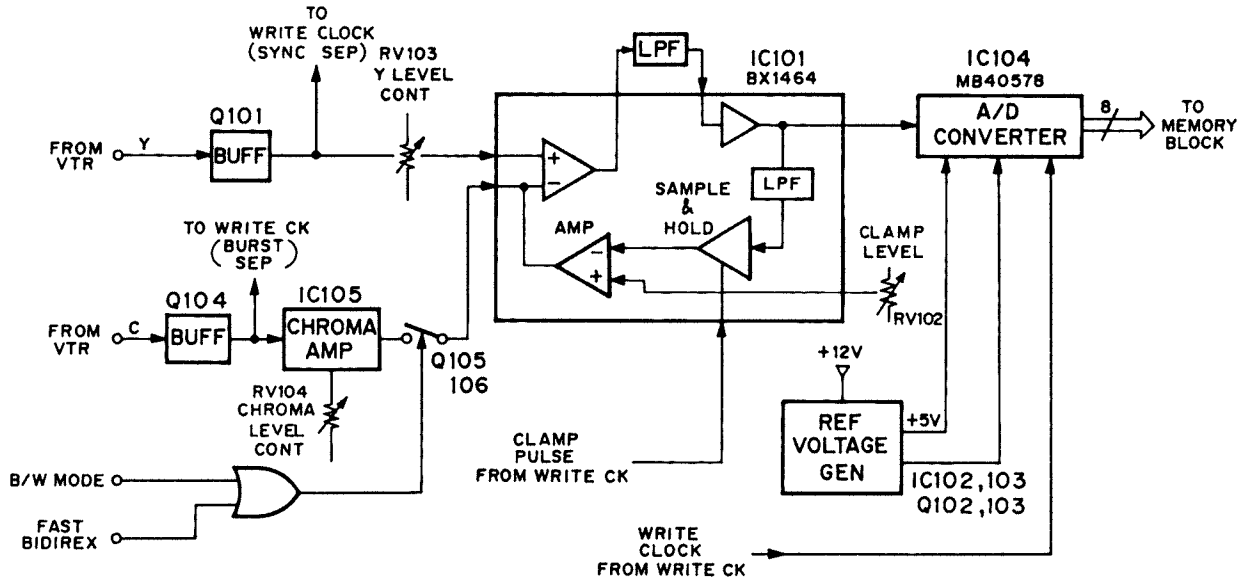


Fig.7-6. Input Block

7-5-3. A-D Converter

The A-D conversion range is +3 to +5Vdc. The video signal is processed by an A-D converter and clamp circuit so that the conversion range of +145 to −40IRE can be obtained as the reference of the pedestal level.
Fig.7-7 shows the A-D conversion rang at pins 17 and 18 of IC104.

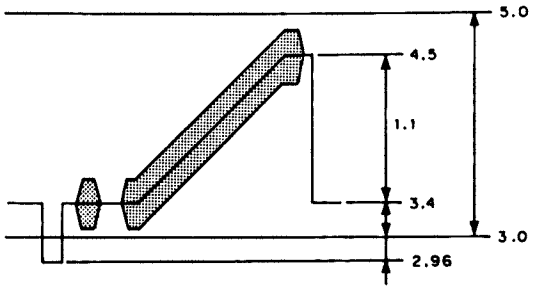


Fig.7-7. A-D Conversion Range

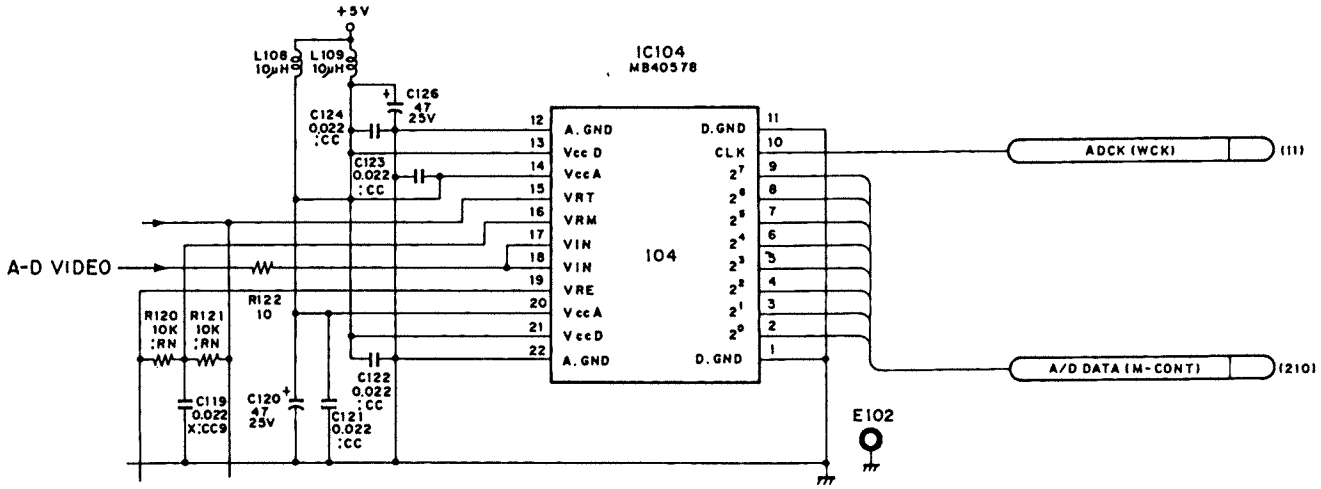


Fig.7-8. A-D Converter Circuit

7-6. MAIN MEMORY

Fig.7-9 shows the main memory block diagram. The 8-bit data (WRITE DATA) which is passed through a dropout compensator and sent at WRITE clock timing is serial-to-parallel converted into 8 phases by using a serial-to-parallel shift register IC404 and 411. IC404 and 411 latch the 8-phase parallel output data at 1/8-WRITE clock timing and write them into the main memory.

The main memory, provided with 8 RAMs having a capacity of 2k×8 bits and an access time of 55nsec, consists of a 16-line memory. The window is 15Hp-p. The 8-bit data which is read from main memory is latched and sent to the D-A converter.

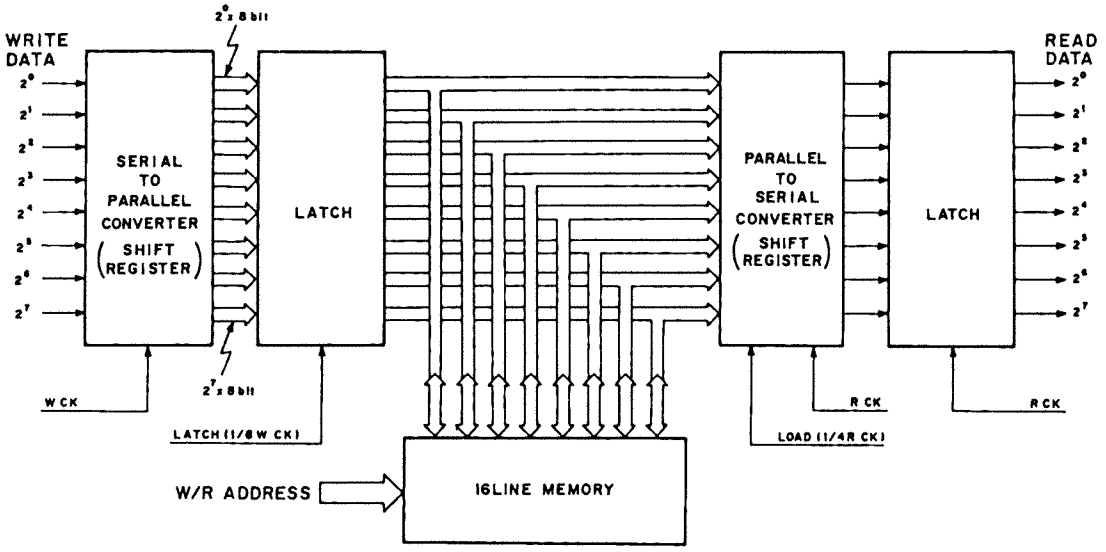


Fig.7-9. Main Memory Block

7-7. DROPOUT COMPENSATOR

The A-D converted video signal is input to the dropout compensator as 8-bit data. In this unit, dropouts in both the Y and chroma signals are compensated for by partial replacement of 1H before. As far as the chroma signal is concerned, the subcarrier phase is inverted every 1H due to the interleaving relationship and so, for this reason, the Y signal system and chroma signal system are characterized by separate processing. As a result, a Y/C separator is required. The dropout compensator uses a digital filter to separate the Y and chroma signals.
The signal of 1H before which is stored in the 16-line memory passes through the parallel-to-serial converter inside IC404 and 411, it is read out at all times, it passes through the chroma inverter and Y/C separator inside IC403, and its dropouts are compensated.

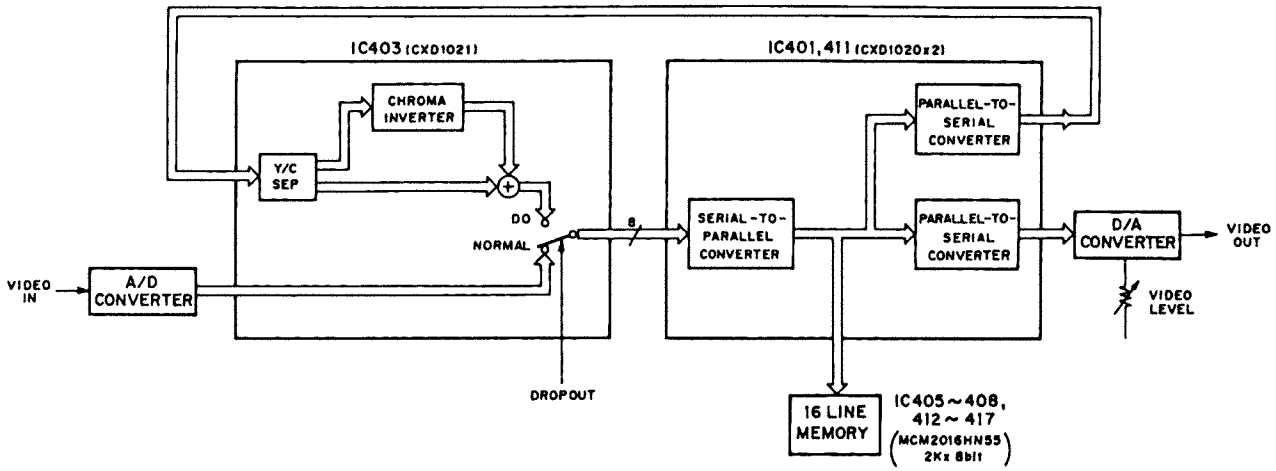


Fig.7-10. Dropout Compensator and Memory

7-8. D-A CONVERTER

The 8-bit data which is read from the main memory is input to the D-A converter.
Video level control is carried out by changing the voltage VREF of the D-A converter.

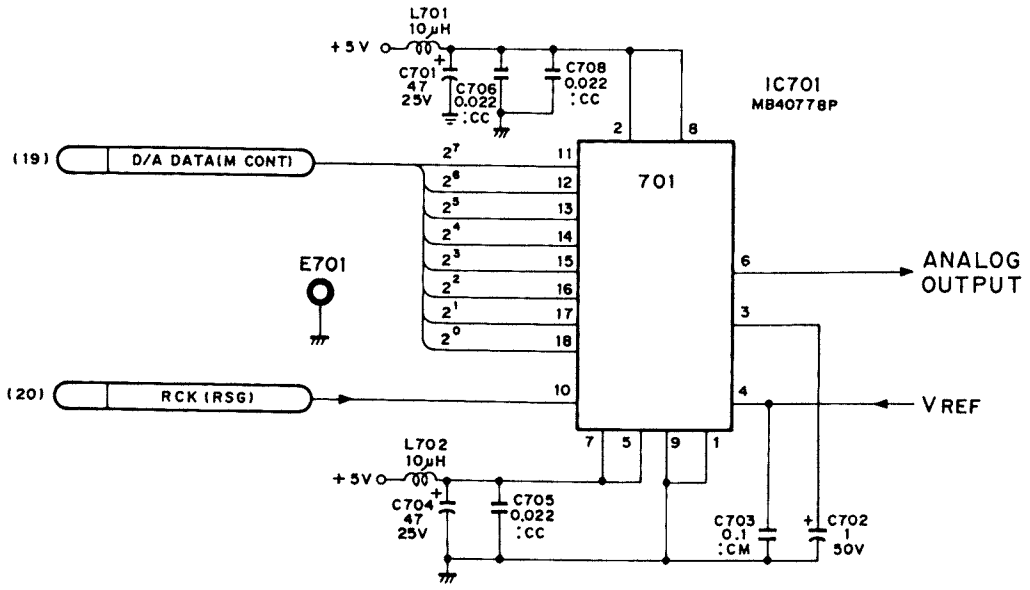


Fig.7-11. D-A Converter

7-9. SECONDARY BEAT CANCELLER

A secondary beat means that the beat components, which are double the frequency of the low-frequency conversion chroma signal (688kHz) which occur in the Y signal because of the characteristics of the electromagnetic conversion system.

In the BVU-850, this circuit was provided on the video board of the VTR, but with the BVU-950 it is provided inside the BKU-901.

Since secondary beat is a kind of chroma signal components, their phase relationship is inverted line by line. These components are detected by subtracting them from the signal of one line before using a 1H delay line. In this circuit, the Y signal without vertical relation against the secondary beat component is output ; moreover, the Y signal without relation is removed and the secondary beat component only is extracted. This output is mixed with the D-A converted main line signal so that the secondary beat is cancelled from the main line signal. The D-A converted video signal is divided into two paths and it is input to FL601 and FL701. The chroma component (3.58MHz) is removed by FL601. The signal then passes through the buffer IC601 and amplifier, it is delayed by approximately 1H by the CCD IC604, and the CCD clock component is filtered out by the low-pass filter FL602. The amount of delay is then adjusted accurately by Q604 and RV605, the level is adjusted by RV606, and the secondary beat is cancelled out by mixing the resulting signal with the main signal at the base of Q608. In order to eliminate the Y high-range components, the signal is passed through the high-pass filter R664 and L603 and the limiter IC602, and it enters the switcher Q610 and 611. The limiter output is passed through the secondary beat trap circuit, it is full-wave rectified by IC603, Q626 and Q627, and it controls ON and OFF of the switcher as identifier signal without relation for the Y signal.

Q606 is turned ON in the EE mode, B/W mode and FAST BIDIREX mode, and the secondary beat canceller is turned OFF. This circuit is forcibly turned OFF by setting S601 on the BKU-901 to OFF. The secondary beat components are mixed with the Y main signal that is passed through the FL701, by the base-grounded amplifier Q619 and cancelled out.

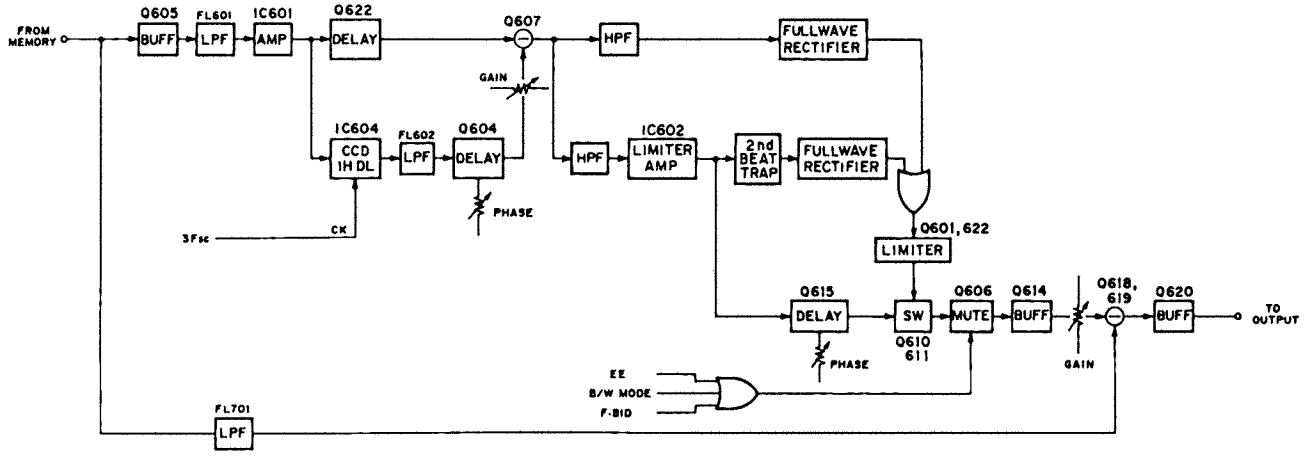


Fig.7-12. Beat Canceller

7-10. PROCESSOR

7-10-1. Pedestal Clamp Circuit

The signal output from the secondary beat canceller circuit is supplied to IC711 (BX1455) where the pedestal is clamped.
A feedback type of clamp circuit is contained inside IC711. The pedestal potential is sampled and held by the READ CLAMP pulse and the resulting error voltage is negatively fed back to the operational amplifier located inside IC711. The clamping potential can be varied by using the TBC remote controller BVR-55 in order to control the setup level.
Pedestal clamped signal is input to the dark clip circuit where the noise below the pedestal level is reduced.
The frequency response is then compensated for by the aperture compensator.

7-10-2. Blanking and Burst Adder

The pedestal clamped video signals is input to the blanking and burst signal adder via the dark clip circuit.
This blanking circuit is contained inside IC711 where the blanking and burst signal mixing operations are performed simultaneously by selecting the input video signal and the new waveform-shaped burst signal.
The reference subcarrier (PROC SC signal) sent from the READ SG is used as the newly added burst signal.

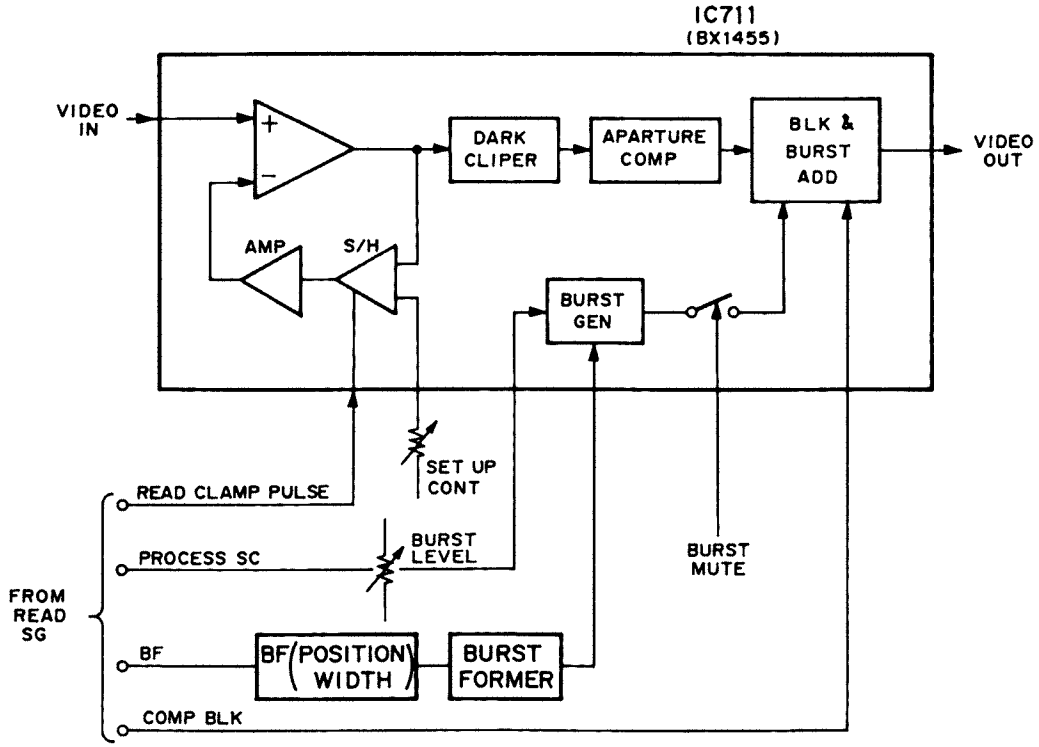


Fig.7-13. Pedestal Clamp Circuit

7-11. VIDEO OUTPUT CIRCUIT

Fig.7-14 is a block diagram of the video output circuit.

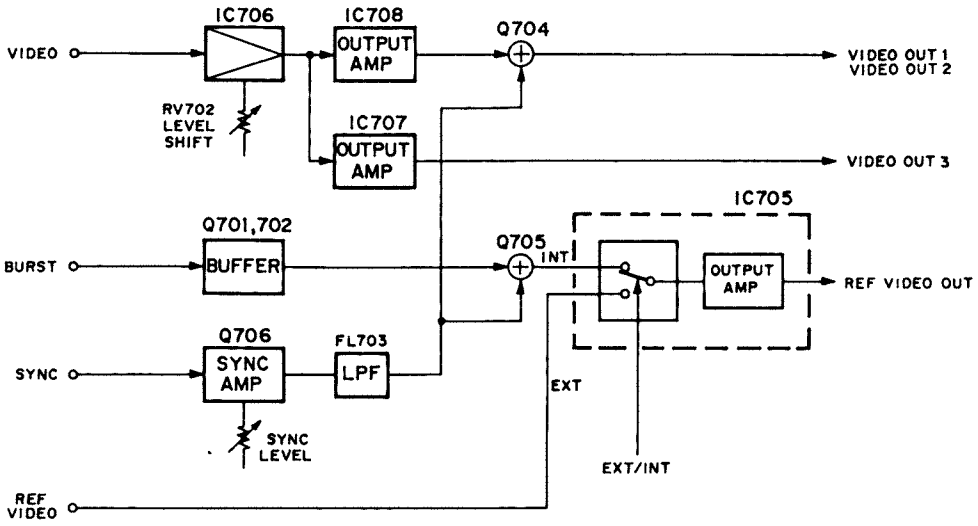


Fig.7-14. Block Diagram of Video Output Circuit

7-11-1. Output Buffer

The video signal output from the processor circuit is fed to an output amplifier consisting of IC706 through IC708. Fig.7-15 shows the output buffer circuit.

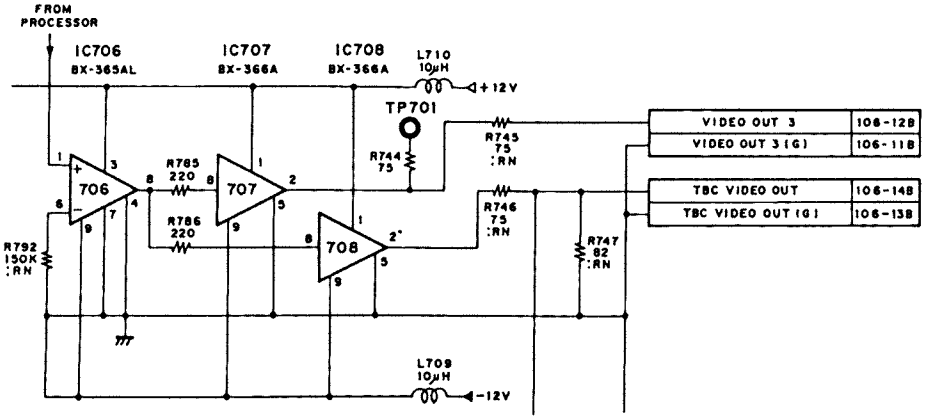


Fig.7-15. Output Buffer

7-11-2. Sync Addition Circuit

The video signal output from an output buffer is output with the sync signal added in the final stage. Fig.7-16 shows the sync addition circuit. This circuit consists of Q704 through Q706.
The reference sync signal input to this circuit is adjusted by RV708 and output from the collector of Q706. Thereafter, the output signal is passed through the next-stage FL703. Then, the reference sync is waveform-shaped in this filter and input to the output transistors Q704 and Q705.

7-11-3. Black Burst Generator Circuit

The burst signal is output from pin 9 of IC711 and it is tuned with LV701. This signal is fed back to pin 10 of IC711 with Q701. On the other hand, tuned burst signal is level-controlled by Q702, sync signal is added by Q705 so that the black burst signal is generated.

7-11-4. Reference Video Output Circuit

When any signal is input to the REF VIDEO IN connector, input signal is output from the REF VIDEO OUT connector.
However, when no signal is input to the REF VIDEO IN connector, the black burst signal is output from the REF VIDEO OUT connector. The selection and output of above conditions are carried out by IC705.

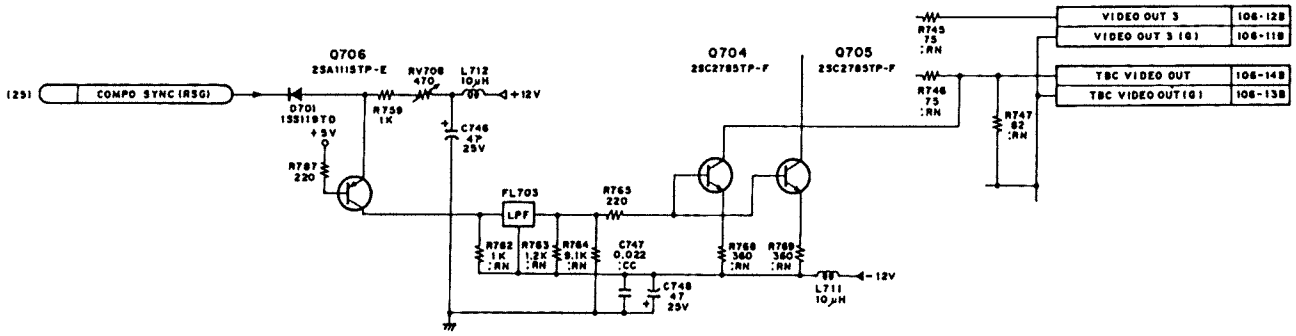


Fig.7-16. Sync Addition Circuit

7-12. WRITE SYSTEM

7-12-1. Sync Separator

The playback video signal from the video circuit is divided into one signal which is supplied from the Q101 buffer output to the sample & hold circuit for A-D conversion and into another signal which is supplied to the sync separator. The video signal which is fed to the sync separator is removed its undesirable high-frequency components by a low-pass filter composed inside IC318, and is distributed to the sync separation sub-circuit and the sync separation main circuit. The sync separation sub-circuit generates the clamp pulse for the sync separation main circuit.
Since the playback signal contains dropout and noise or pedestal level fluctuations. In order to prevent above influence, clamping of the sync separation main circuit is prohibited in such case.
Only the H SYNC signal which is removed their pseudo sync due to noise is extracted from the generated PB SYNC signal by the SELECT H circuit.

7-12-2. Select H Circuit

The SELECT H signal is a periodic H sync pulse extracted from the PB sync. The PB sync signal is separated from the playback output signal and sent to this circuit. The PB sync signal usually has periodicity, but dropouts and some other factors may occasionally cause the PB sync signal to be a periodic. Since WRITE clock and other signals are generated from the PB sync signal, the SELECT H generator must select the periodic H sync signal from the PB sync signal.
The SELECT H circuit is configured inside IC415 (CXD1023AQ).
The PB sync signal is input to pin 2 of IC415 and the H periods are counted by the 4fsc clock supplied to pin 63 (HCK). A window for extracting the H SYNC is provided by the count data and only the H SYNC inside this window is output as the GATED H signal from pin 58 (GH). From pin 53 (GB) is output a low signal starting from the time the H SYNC signal is not output as the GATED H signal and ending when the next GATED H signal is output. The window width of the GATED H signal in this circuit is approximately 1 μ s.

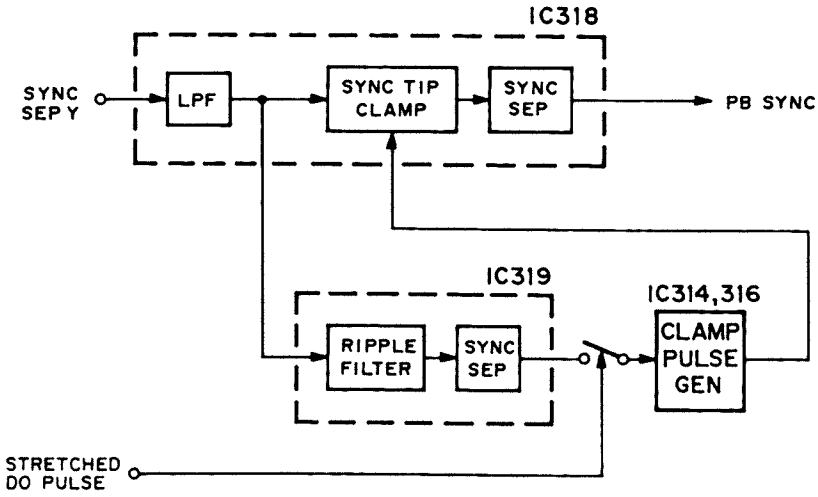


Fig.7-17. Sync Separator

7-12-3. Write Clock Generator

The WRITE clock is synchronized with the playback video signal and is used as the reference signal for A-D conversion and for writing digital data into the memory.

The WRITE clock is generated by the automatic frequency control (AFC) circuit using the SELECT H signal. Fig.7-18 shows the block diagram of the AFC circuit. The AFC circuit is an AFC loop consisting of a 4fsc VCO, a 1/4-counter, a 1/910-counter, a sawtooth signal generator and a sample-hold circuit.

The output of the VCO is fed to the 1/910-counter where its frequency is divided by 910 to form the H period pulse. This pulse is called the COUNTER H signal and it generates a sawtooth signal. The sawtooth voltage is sample-held by the SELECT H signal. The sample-hold circuit output is used to control the frequency of the VCO. Thus, the VCO oscillates in synchronization with the SELECT H signal. A window is formed by IC317 at the sample & hold output section, and only when the SELECT H signal is in this window, the sawtooth voltage is sampled and held.

The AFC circuit contains two VCOs. One operates in the FAST BIDIREX mode, and the other operates in the other mode. The FAST BIDIREX VCO has a center frequency of 4 fsc with a variable frequency range of more than +50% of 4fsc. This VCO follows in the FF or REW mode for the U-matic VTR. This type of VCO is rather unstable because of its wide frequency range. In the normal PB or SLOW BIDIREX mode, another VCO operating in a narrow variable frequency range of ±10% with high frequency stability is used.

The output of the VCO at 4fsc, which is fed from the stabilized AFC loop, is output as the WRITE clock.

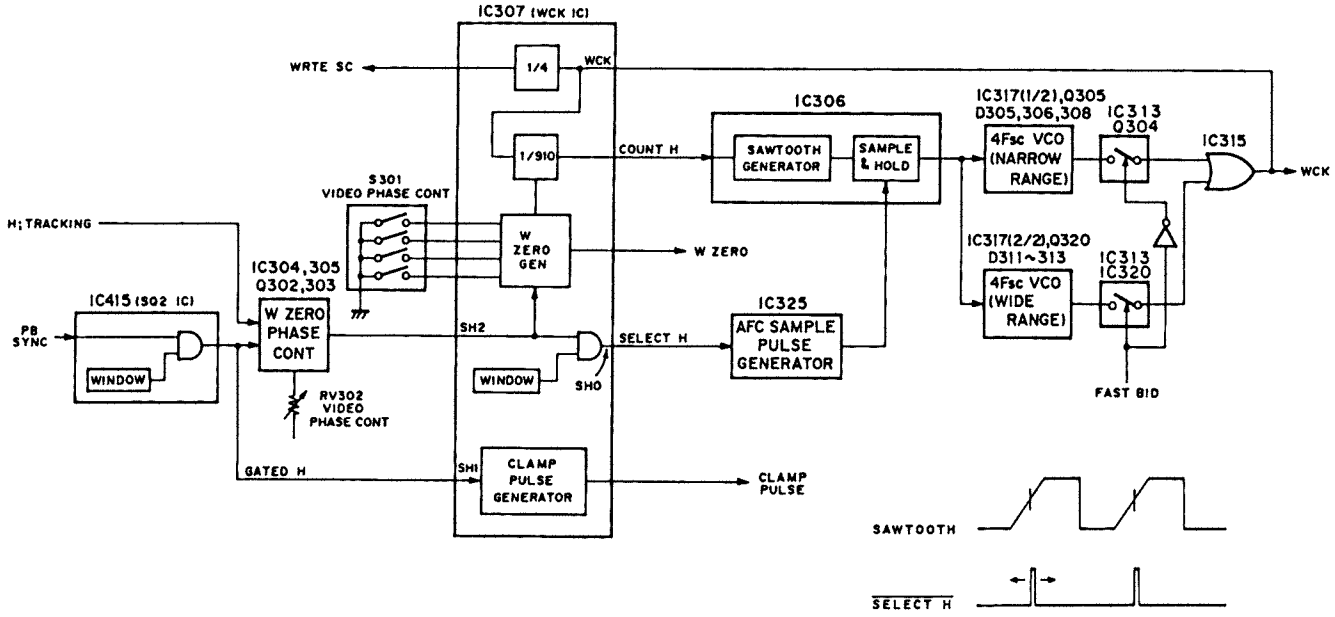


Fig.7-18. Write Clock Generator

7-12-4. Write Zero Pulse Generator

WRITE ZERO is a narrow-width pulse. It is synchronized with COUNTER H which is generated by dividing the VCO output by 910 in the AFC loop. WRITE ZERO is used to clock the WRITE line address counter and to reset the WRITE address counter.

7-13. SYNC DELAY SWITCH

In the TBC, normally, the video signal whose time base has been corrected is output in synchronizing with the reference signal during playback mode.
In the EE mode, the video signal phase is delayed for 8H. The sync signal which is added to the 8H delayed video signal can be controlled whether delaying for 8H or in-phasing to the reference signal phase. Above selection is performed by switch S402. Normally S402 is set to 8H.

7-14. INT (Plug-in) TBC BYPASS/ON/AUTO SWITCH

Internal TBC ON/OFF switch is located in the lower side of the BVU-950. Function of this switch are as follows.

SWITCH POSITION	MODE	
	EE	PB
BYPASS	TBC-BYPASS	TBC-BYPASS
ON	TBC-ON	TBC-ON
AUTO	TBC-BYPASS	TBC-ON

7-15. READ SYSTEM

7-15-1. Ref. Sync Signal Generator

Fig.7-19 is a block diagram of the reference sync signal generator.
The unit is lock to the external signal when an external reference video signal is input. The VCO oscillating at 4fsc is locked to the external sync signal obtained by separating the sync signal from the input reference video signal. The clock signal is fed from the VCO to IC511 and IC514 to generate the reference sync, VD, HD and the other signals. The HD signal output from IC511 is compared with the sync signal obained from the external reference video signal by using a phase comparator in the reference sync signal generator. The 4fsc VCO is controlled by the obtained error voltage. Thus, the FH signal is always locked to the external reference video signal. The phase shifter (IC504, 506) in a feedback loop is used to adjust the phase delay of the H sync signal by using the H PHASE signal across a range from -1 to $+3\,\mu$sec. When no reference video signal is input, this unit operates in the INT mode. Either the EXT or INT mode is selected when IC505 detects whether a sync signal is being input or not. The 4fsc VCO is controlled by the voltage set by RV501 in the INT mode.
In the next stage, READ clock, READ ZERO, sync and blanking pulse signals are generated to control the READ system by using the reference signal generated in the reference sync generator.

7-15-2. Blanking Circuit

This circuit generates the H and V blanking pulses. This circuit is composed of IC511, 514 and 515.
During vertical blanking, the circuit generates a pulse corresponding to the 10th line, based on the VD and HD pulses from the sync generator IC514, inside the blanking width controller IC515. This pulse is delayed by the shift register in 1H steps to generate the vertical blanking pulses in the 10th through 21st lines. Blanking ON/OFF for each line can be controlled by switches S503 and S504. During the vertical sync equalizing pulse period, the VD pulse is output without modification as the blanking pulse. The 1/2H-width blanking pulse is required to generate the video signal at the 1/2H position in the second field. The 1/2H-width blanking signal is generated from both the odd/even signal fed from the reference sync generator and 20th-line blanking signal by using IC512, 513 and 524. The blanking pulse is not normally fed in the 21st line when switch SW502 is in the OFF position. The blanking pulse continues to the 1/2H position on the 20th line in the second field.

7-15-3. Read Clock Generator

The READ clock is used as a clock pulse to read out the digital video signal from the memory.
The WRITE clock pulse frequency is 4fsc and so the READ clock pulse frequency is also 4fsc. The READ clock pulse is generated from the stable reference signal, compared with the WRITE clock pulse, and so the circuit involved is relatively uncomplicated.
Fig.7-19 shows the block diagram of the READ clock generator. The READ clock is generated from the 4fsc VCO output locked to the reference burst of the EXT reference video signal.

When no EXT reference video signal is input in the INT mode, clock generated by the crystal oscillator X502 is used as READ clock and the clock for generating the sync signal. The subcarrier phase control circuit is part of the VCO gen-lock loop so that the subcarrier phase of the output video signal can be controlled. The VCO output is divided by 4 and use as the process SC signal, so that it is replaced with the PB burst after D-A conversion is carried out.

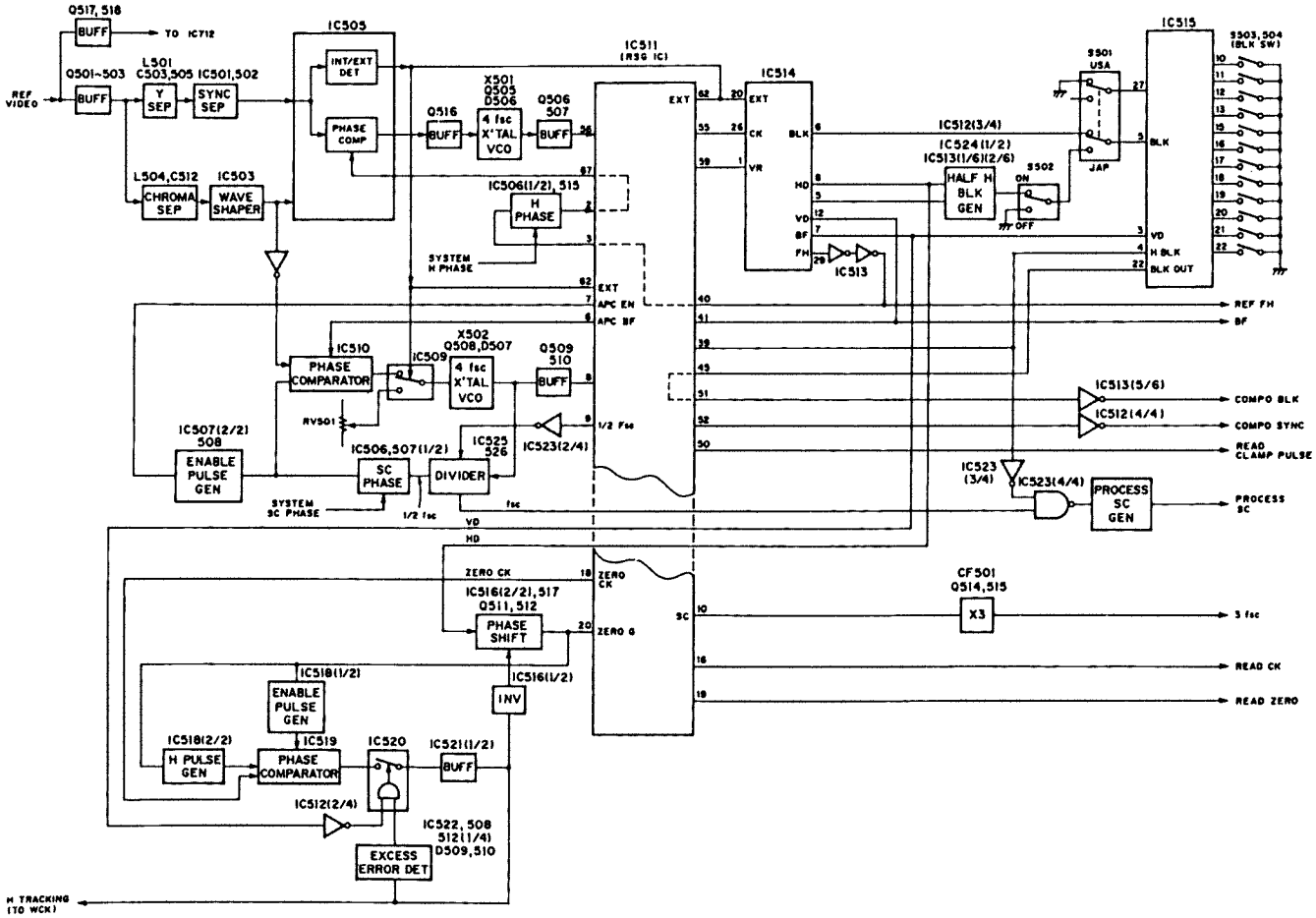


Fig.7-19. Read Clock Generator

7-15-4. Read Zero Pulse Generator

The READ ZERO pulse indicates the start of main memory reading. The READ ZERO pulse is generated by synchronizing the HD signal from the reference sync generator with fsc. The 4fsc VCO output, which can be used to generate the READ clock, is divided by four to generate fsc in the READ system.
The READ ZERO phase is shifted minutely by the SC PHASE or H PHASE control on the remote controller. The READ ZERO phase shift is offset by feeding it back to the WRITE ZERO signal generator in the WRITE system. The phase error information that feed back to the WRITE ZERO generator is called the H TRACKING.

7-15-5. Write/Read Address Generator

The 8-bit WRITE data ($AD2^0$ through $AD2^7$) sent in synchronization with the WRITE clock timing are converted into 8-phase parallel data by the serial-to-parallel converter IC404 and 405. The 8-phase parallel data is stored in the main memory which has a capacity of 16H. The main memory consists of eight static RAMs, each having a capacity of 2048-word × 8-bit. The RAM address ($MA2^0$ through $MA2^{10}$) is controlled by the WRITE/READ line address (2^0 through 2^3) and specifies one line of 16H. An address within 1H is specified by A0 through A6 of the RAM. In address generation, the counter is reset by the WRITE ZERO or READ ZERO signal. Thereafter, the counter is operated by the 1/4 WRITE clock or 1/4 READ clock to generate the address.

7-15-6. Fast Bidirex Detector

The fast BIDIREX (high-speed playback) detector circuit is contained inside IC415.
With variable speed playback, the color signal is output up to ±5 times normal tape speed by the TBC, and if the speed is any higher, a B/W signal is output. The mode with a speed above ±5 times normal tape speed is called as fast BIDIREX.
In order to detect the playback speed of the VTR, the H interval data of the GATED H signal is compared with the reference value inside IC415.
In the fast BIDIREX mode, a low-level signal is output from pin 55 of IC415 ; in the fast reverse BIDIREX mode (high-speed reverse playback), a low-level signal is output from pin 56.

SECTION 8
TIME CODE SYSTEM

8-1. OUTLINE

The time code system of the BVU-950 consists of time code signal recording and playback amplifiers on the BC-11 board. During recording, the signal from the external time code generator, which is supplied to the TIME CODE IN connector on the rear panel, is recorded onto the tape. The played back time code is amplified by the playback amplifier and output from the TIME CODE OUT connector.
When the optional BKU-905 (time code generator/reader) is installed in the BVU-950, the SMPTE time code signals generated by the BKU-905 are recorded onto the address track on the tape when VTR recording is performed. During VTR playback, the time code on the tape is read out, it is displayed on the VTR's time counter and at the same time it is output as the SMPTE time code signal from the TC OUT connector.

8-2. FEATURES

The features of the BKU-905 are listed below in the form of a comparison with the BK-806 time code generator/reader for the BVU-800 series.

ITEM	BKU-905	BK-806
READER	Yes	Yes
GENERATOR	Yes	Yes
TIME CODE/U-BIT PRESET	Yes	No
FREE RUN/REC RUN	Yes	Yes
DF/NON-DF (NTSC only)	Yes	Yes
TC GEN SLAVE LOCK	Yes	No
TC CHARACTER SUPERIMPOSE	Yes	No
VITC	No	No
TC INSERT	No	No

Table 8-1. Features

• Time Code/User Bits Preset
With the BK-806, the data can not be preset at the VTR side for both the time code and user's bit. In contrast, with the BKU-905, the data can be set for the time code and user's bit at the front panel using dial menu operations.
(Reference should be made to the system control section for details on the dial menu.)

• FREE-RUN/REC-RUN Selection
With the BK-806, this selection was done by a switch on the circuit board inside the BK-806. In contrast, with the BKU-905, it can be done using a switch located underneath the front panel. This is a feature which enhances operational ease.

• Drop Frame/Non-drop Frame Selection
(For NTSC only)
With the BK-806, this selection was done by a switch on the circuit board inside the BK-806. In contrast, with the BKU-905, it can be performed by a dial menu operation using the jog dial on the front panel.

• Time Code Generator Slave Lock Function
In the past, if the same time code as the playback time code from another player was recorded onto a VTR, the resulting dubbing gave rise to a deterioration in the time code when the signal supplied to the TIME CODE IN connector was recorded as is.
The BKU-905 has a slave lock function for locking the generator to the time code supplied to the TIME CODE IN connector and it enables the time code which has been generated again by the generator to be recorded (REGEN function). As a result, time code signals without any of the deterioration caused by dubbing can be recorded.

• Time Code Character Superimpose Function
During recording, the BVU-950 enables time code characters to be superimposed onto the video signals and recorded, and during playback it enables them to be superimposed onto the video signals and output from the monitor video output connector. The selection of the superimpose function is controlled by the CHARACTER ON/OFF switch located underneath the front panel.

8-3. TIME CODE SIGNAL FORMAT

The SMPTE time code signal format is shown in Fig. 8-2. The time code signal has one address in every frame. The address consists of 80bits. Among one frame, a 4-bit binary word are placed alternately in 64 bits, and the remaining 16bits make a sync word. The basic configuration of the time address is based on a BCD code. Since a "10" digit does not require a 4-bit BCD code, two bits are used to display "hour" and "frame", and three bits are used to display "minute" and "second". 32-bits (4bits×8) of the binary word can be used as user bit information. The 16-bit sync word starts with "00", then is followed by "1" from the 3rd bit through the 14th, and ends with "01". This enables detecting whether the tape is running in the forward or reverse direction. In other words, when the sync word starts with "00", the tape is running in the forward direction, on the other hand with "01", the tape is running in the reverse direction.

As shown in Fig.8-1, the time code signal starting position is synchronized with the "leading edge +1H of the third wide pulse" of the vertical sync signal.

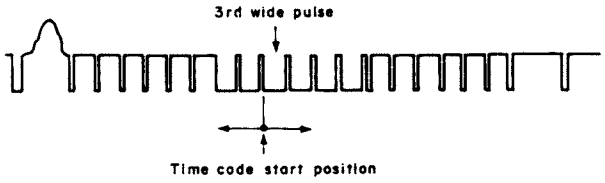


Fig.8-1. Time Code Starting Position

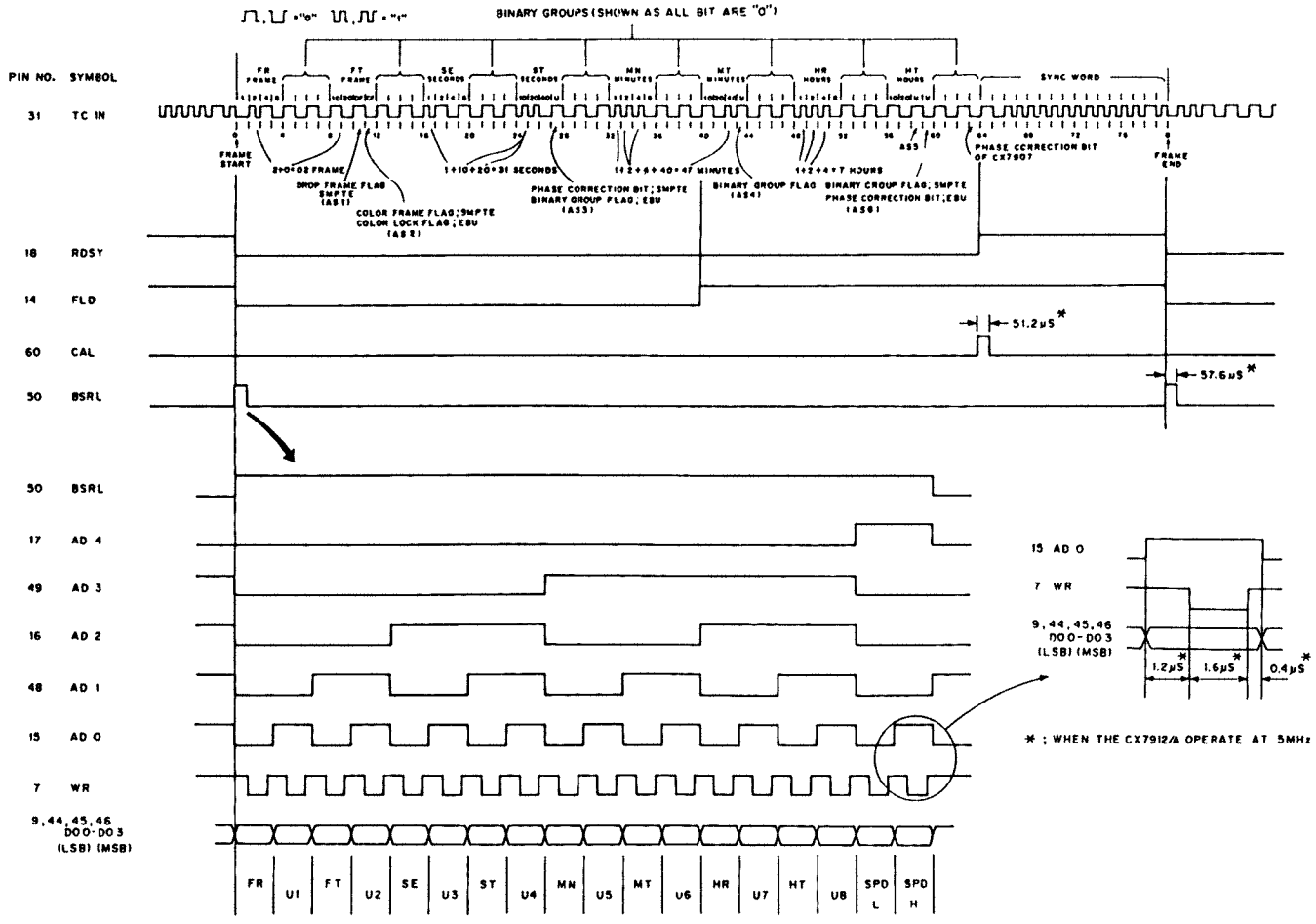


Fig.8-2. Time Code Signal Format

8-4. TIME CODE SIGNAL MODULATION SYSTEM

The BKU-905 uses a Bi-phase mark modulation system to modulate the time code signal. This system has the following features :

- A transient occurs at the starting edges of every bit period.
- "1" means that a transient occurs in the middle of bit period.
- "0" means that a transient occurs at both the starting and ending edges of a bit period.

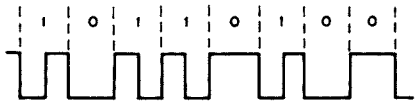


Fig.8-3. Bi-phase Mark Modulation System

8-5. DROP FRAME

Drop frame corrects for the time difference between real time and the color video signal time. An NTSC color video signal scans 29.97 frames per second. The result is a frame difference of 108 frames (0.03×60 ×60) per hour. To correct this frame difference, two frames, 00 and 01 frames, are not counted at the starting position (i.e. at 3 minutes 00 seconds 00 frames) of every minute except the 00, 10, 20, 30, 40 and 50th minutes.

In 00H 18M 59S 29F shown as example (A), the "minute" digit cannot be divided by 10. Therefore, the 00 and 01 frames are not counted. After 18M 59S 29F, 19F 00S 02F is displayed.

In 01H 20M 00S 00F shown as an example (B), the "minute" digit can be divided by 10. Therefore, drop frame is not performed. After 01H 19M 59S 29F, 01H 20M 00S 00F is displayed (and then 01H 20M 00S 01F).

In 12H 20M 59S 29F shown as an example (C), the "minute" digit can also be divided by 10. Therefore, drop frame is not peformed. After 12H 20M 59S 29F, 12H 21M 00S 00F is displayed. As a result, correction is performed 54 times (60−6=54) per hour. In other words, 108 frames are corrected per hour.

Moreover, in the drop frame mode, the time code generator sets the 10th bit of each address as "1". This bit is used as a drop frame flag.

Example :

(A)	(B)	(C)
00^{H} 18^{M} 59^{S} 29^{F}	01^{H} 19^{M} 59^{S} 29^{F}	12^{H} 20^{M} 59^{S} 29^{F}
	01 20 00 00	12 21 00 00
	01 20 00 01	
00 19 00 02	01 20 00 02	

8-6. PHASE CORRECTION BIT (PARITY BIT)

In the biphase-mark modulation system used for time code addresses, it is impossible to determine whether the 0th bit starts at the raising or falling edge (when there are an odd number of 1s in 80-bit address, the relationship between the raising and falling edges is reversed at the 0th bit of the 80-bit address and 0th bit of the next 80-bit address). Controlling whether a particular bit is set as "1" enables the 0th bit to start at the falling edge. In an NTSC signal, the 27th bit is used as the phase correction bit.

8-7. BC-11 BOARD

Fig.8-4 is a block diagram of the BC-11 board.

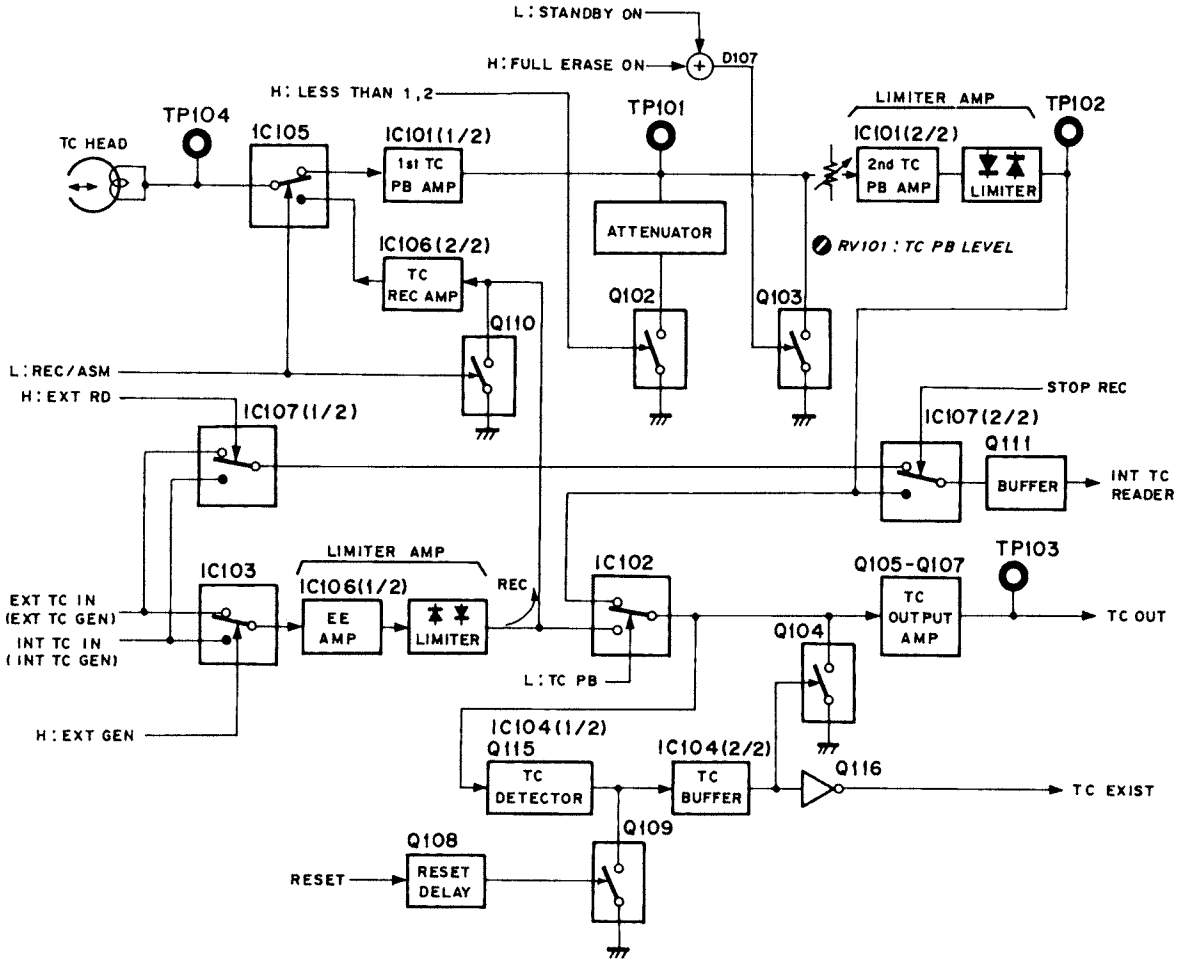


Fig.8-4. BC-11 Board

8-7-1. Input Amplifier

The external time code signal fed to the TIME CODE IN connector on the connector panel is input to terminal 6A on the BC-11 board. The internal time code signal generated by a time code generator on the BKU-905 is also input to terminal 8A on the BC-11 board.
These signals are first sent to the TC EXT/INT SELECT switcher IC103 and then they are amplified by the TC input amplifier IC106 (1/2).

8-7-2. Control Logic Circuit

This circuit is a logic circuit, and controls the time code signal amplified by the input amplifier and the time code signal played back with the time code playback head.
The following three signals are input to this control logic circuit.

1. Data from the external time code generator connected to the TIME CODE IN connector on the connector panel.

2. Data from the internal time code generator of BKU-905.

3. Data reproduced by the TIME CODE R/P head

ON the other hand, this circuit has the following three outputs.
(1) Data to the external time code reader that is output from the TIME CODE OUT connector on the connector panel
(2) Data to the internal time code reader that is output to the time code reader of BKU-905.
(3) Data to the time code head for recording.

These inputs and outputs shall be explained in the following.

(1) Signals Output to the External Time Code Reader
As shown in Table 8-2, the output signal is selected by the PRESET/SLAVE LOCK and EXT/INT switches on the front panel of the BVU-950 and by the operating mode (PB/REC/EE) of the VTR. The table shows that when, for instance, the INT mode (using the time code generator on the BKU-905), PRESET mode and recording mode is established, the data from the internal time code generator is output to the external time code reader (through the TIME CODE OUT connector on the connector panel).

The data on the tape played back by the time code head is generally used in the playback mode.
However, for the locations marked with an asterisk (*), the data recorded on the tape are read out once at the time code head and then data which is identical to this data is generated by the internal time code generator. Consequently, the data recorded on the tape enables the output to be kept in peak condition by means of waveform shaping, even if unsatisfactory data is recorded on the tape.

(2) Signals Output to the Internal Time Code Reader
As shown in Table 8-2, the signal which is output to the internal time code reader is selected by the EXT/INT switch and PB/REC/EE mode. In the playback mode, the time code on the tape is read by the internal reader. In the recording mode, the time codes from the respective generators are read out by the INT/EXT switch setting.

(3) Signals Output to Time code Head for Recording
As shown in Table 8-2, the signal output to the time code head is selected by the EXT/INT switch and PRESET/SLAVE LOCK switches.
As shown in Table 8-2, when the INT mode is selected under the PRESET mode, the data generated by the internal generator is recorded on the tape. When the EXT mode is selected under the PRESET mode, the data generated by the external generator is recorded on the tape. When the INT mode is selected under the SLAVE LOCK mode, the data generated by the internal generator is recorded on the tape. When the EXT mode is selected, the data fed to the TIME CODE IN connector is read once, and then identical data with the output data is generated from the internal generator and output. Consequently, data is recorded on the tape in the optimum condition.

OUTPUT	TC MODE / VTR MODE	INT		EXT	
		INT PRESET	INT SLAVE LOCK	EXT PRESET	SLVAE LOCK
(1) EXT READER	PB	TAPE	INT GEN (PLAY) * TAPE ($\overline{\text{PLAY}}$)	TAPE	←
	REC	INT GEN	←	EXT GEN	INT GEN
	EE	—	—	—	—
(2) INT READER	PB	TAPE	←	←	←
	REC	INT GEN	←	EXT GEN	←
	EE	—	—	EXT GEN	←
(3) REC AMP	PB	INT GEN	←	EXT GEN	←
	REC	INT GEN	←	EXT GEN	INT GEN
	EE	INT GEN	←	EXT GEN	←

EE mode=STOP • REC or ASS • EDIT

Table 8-2

8-7-3. TC Exist Detector/TC Output Muting Circuit

1. TC Exist Detector

The existence of the time code is detected by IC104, Q115, 116, 108 and 109. This time code existence detection is performed by comparing the reference voltage with the signal selected by IC102 in the comparator IC104.

2. TC Output Muting Circuit

The TC output muting circuit in the BVU-950 controls the time code output signal from the TIME CODE OUT connector. Time code output muting is performed using the TC EXIST detector described above.

- When time code exists, the TC output is not muted.
- When time code does not exist, the TC output is muted.

8-7-4. Time Code Output Amplifier

The signal output from pin 1 of the PB/EE switcher IC102 is sent to the TIME CODE OUT connector on the rear panel via the amplifiers Q105 and Q106. The rising and falling edges of the time code output waveform are determined by the specification shown in Fig.8-5.

The capacitors C68 and C115 determines the time code output waveform during playback to satisfy the specification. When the tape speed changes and increases, the time code output waveform changes as shown in Fig.8-6. However, both the SMPTE and EBU standards define only those operations executed in the normal FWD mode. When the tape speed reaches 1.2× the normal FWD speed, C104 is cut off to prevent change in the waveform.

As shown in Fig.8-7, Q102 turns C104 on and off. The output signal of the tape speed detector circuit supplied from the system control circuit serves as the Q102 control signal.

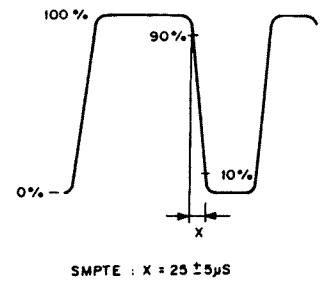


Fig.8-5. Specifications of Time Code Output Signal

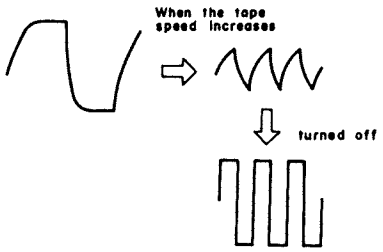


Fig.8-6. Time Code Output Waveform

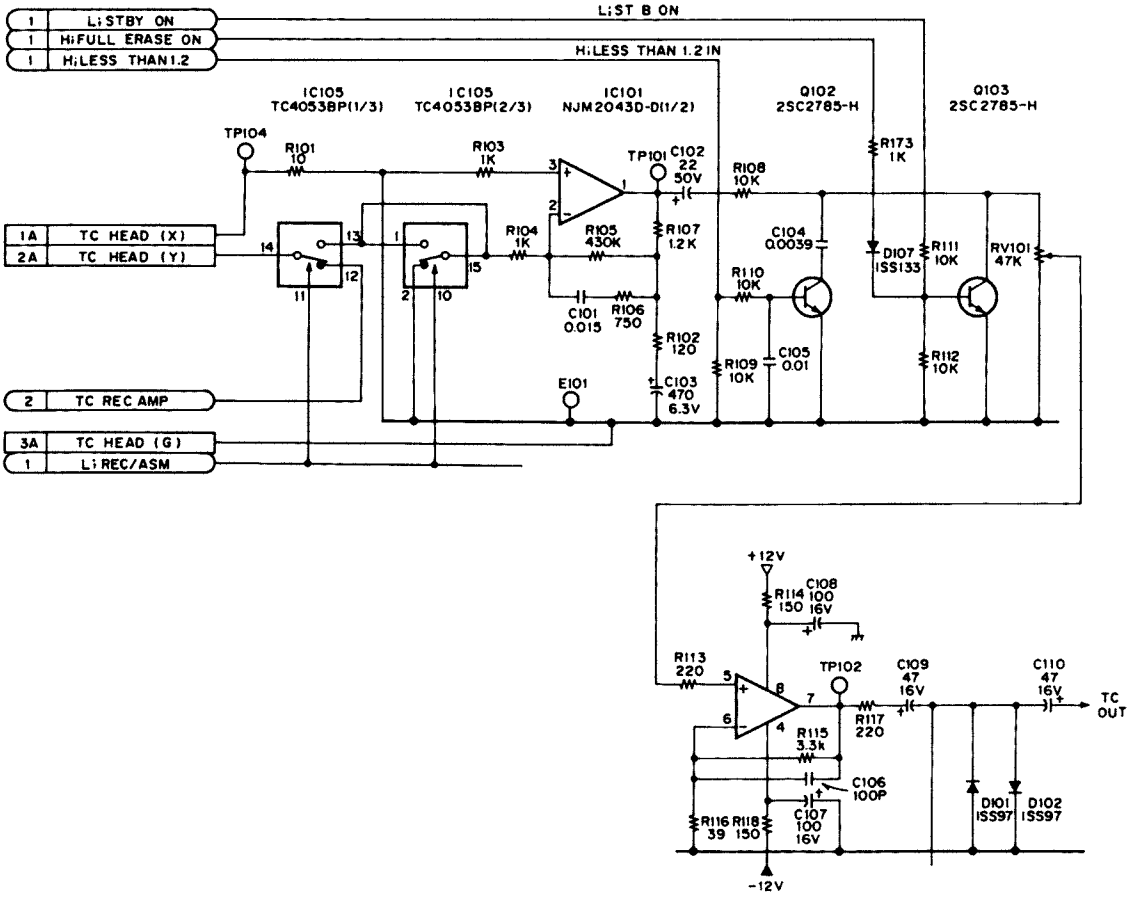


Fig.8-7. Time Code Output Amplifier

8-8. TC-42 BOARD (BKU-905)

Whereas the BC-11 board among the time code system circuits of the BVU-950 is configured with an amplifier circuit, the TC-42 board is composed of a logic circuit. Fig.8-8 is a system diagram of the TC-42 board.

As is clear from the block diagram, the TC-42 board consists primarily of two circuits : the time code generator IC2 and time code reader IC1. Both an 8-bit data bus and 7-bit address bus are used to transfer data to the system control board (SY-102 board).

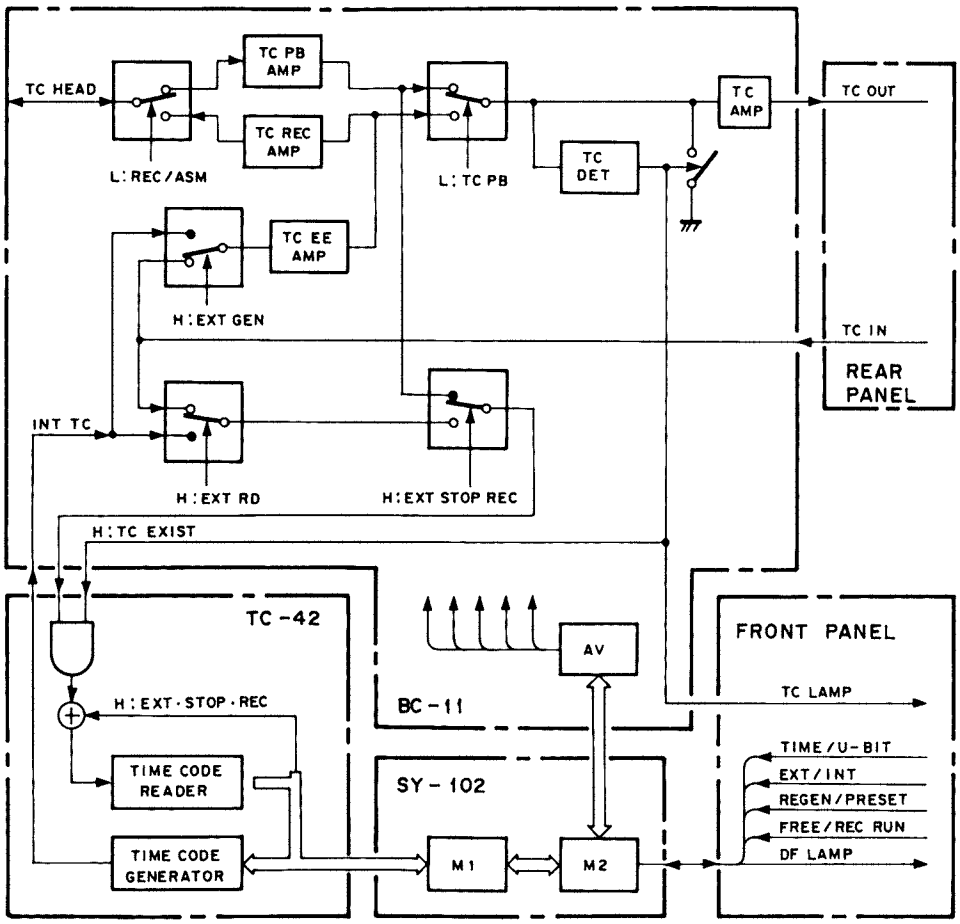


Fig.8-8. Time Code System

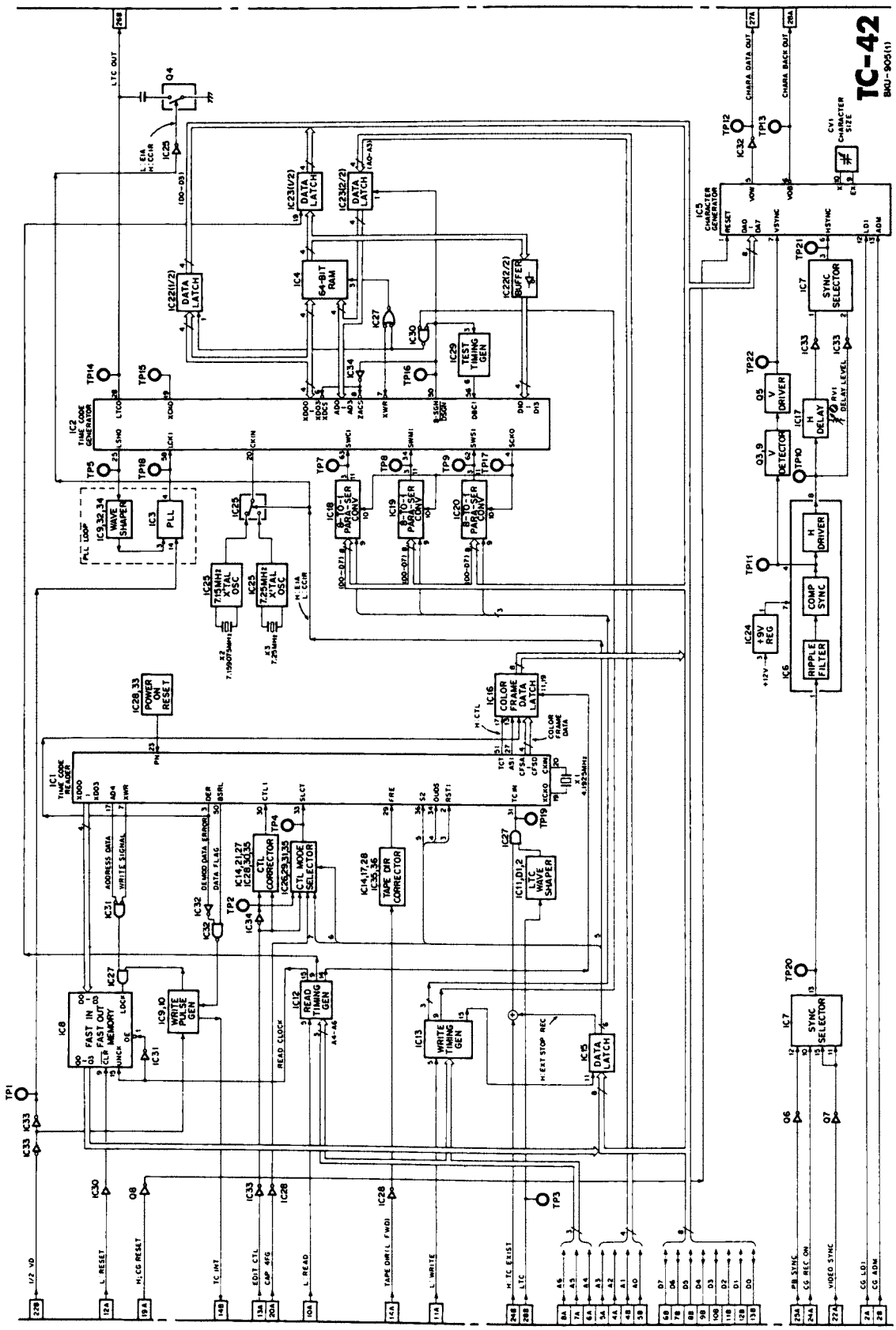


Fig.8-9. TC-42 Board Block Diagram

8-8-1. Time Code Generator Circuit

IC2 (CX7907A) is the time code generator IC. The BKU-905 has two system clock pulses for the time code generator in order for it to be used in common with the EIA and CCIR systems. In the EIA mode, the output of the ×2 oscillator serves as the system clock pulse of the time code generator, and in the CCIR mode, the output of the ×3 oscillator applies. Switching between the two is performed by the data from the microcomputer in the system control section. Control is exercised by the LTC clock pulse, which is input into pin 58 of the generator (IC2), as the time code signal clock pulse. This clock pulse is controlled by the PLL loop which is formed with the reference 1/2VD signal and the time code signal is phase-locked as shown in Fig.8-10.
The PLL circuit is composed of the phase comparator IC3, voltage-controlled oscillator and delay circuit (IC9, IC32).

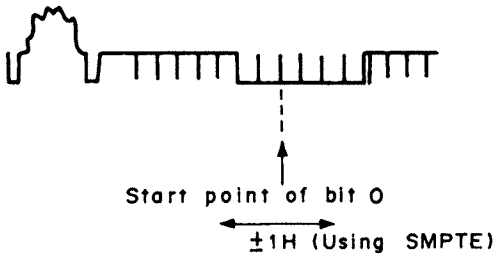


Fig.8-10. Starting Point of Time Code

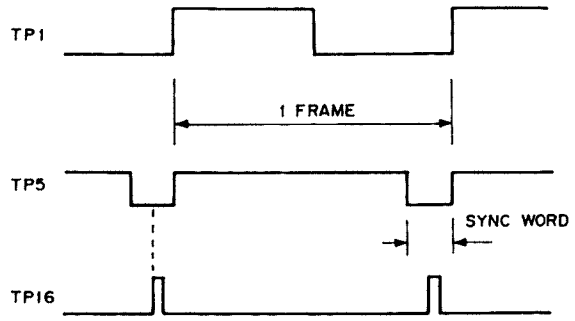


Fig.8-11. Phase Lock

8-8-2. Time Code Reader Circuit

IC1 (CX7912A) is the time code reader IC. Depending on the mode, it reads the CTL signal or time code which is supplied to pin 30 or pin 31.
In the BK-806, the AUTO/TC/CTL switch is on the board but in the BKU-905 these modes are switched automatically.
When the VTR is in the recording mode, IC1 is set to the AUTO mode in which the time code errors are automatically corrected by the CTL signal. When it is in the EE mode, IC1 is set to the AUTO mode. The mode selection of TC AUTO mode and CTL mode is controlled by the result of speed detection of the capstan 4FG. A detection is performed whether the rising edge of the 4FG is existed or not during the particular period from the falling edge of the 4FG. IC26 and IC29 are detector circuit for above purpose. When the speed decreases approximately 0.3 times normal speed or less, mode will be switched to the CTL mode. When the speed increases approximately 0.8 times normal speed or more, mode will be changed to the TC AUTO mode.
Following correction is performed when the mode will be changed to the CTL mode from the TC AUTO mode.

①If the SYNC WORD will be located before the CTL, it will be counted up with next CTL at the timing of CTL mode after the completion of calcuration of the time code with reader. This CTL is corresponded to the preceeding CTL, and already counted up at the TC mode. Therfore, when the mode will be changed into the CTL mode, counting result of reader is subtracted by one for adding the one CTL which is inverted by the preceeding FWD/REV. The other cases, no correction will be carried out.

②If the CTL will be located before the SYNC WORD, and the mode is switched into the CTL mode before calculating the TC, the TC cannot calculate, so count up is not carried out. Therefore, when the mode will be changed into the CTL mode, count up of the reader will be carried out by adding the one CTL depending the previous tape direction. The other cases, no correction will be carried out.

Processing in forward or reverse mode is performed by the IC36 and IC21 is an inverter. Added CTL pulses are generated by IC21 with delaying a little with R117 and C74.

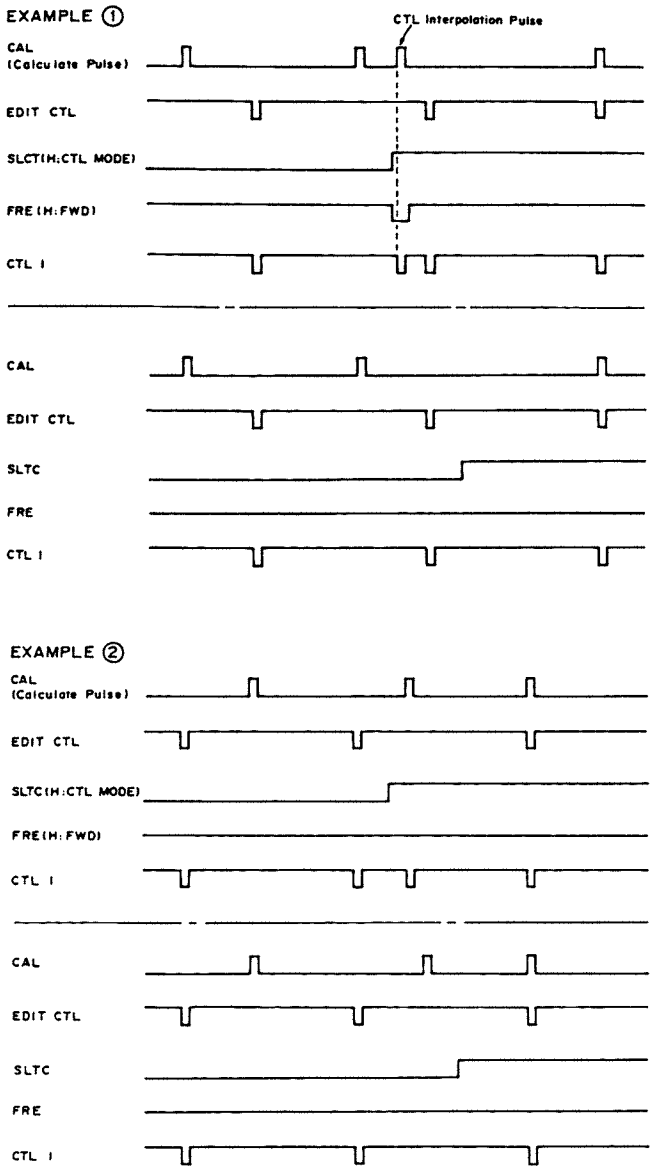


Fig.8-12. Timing Chart of TC Reader

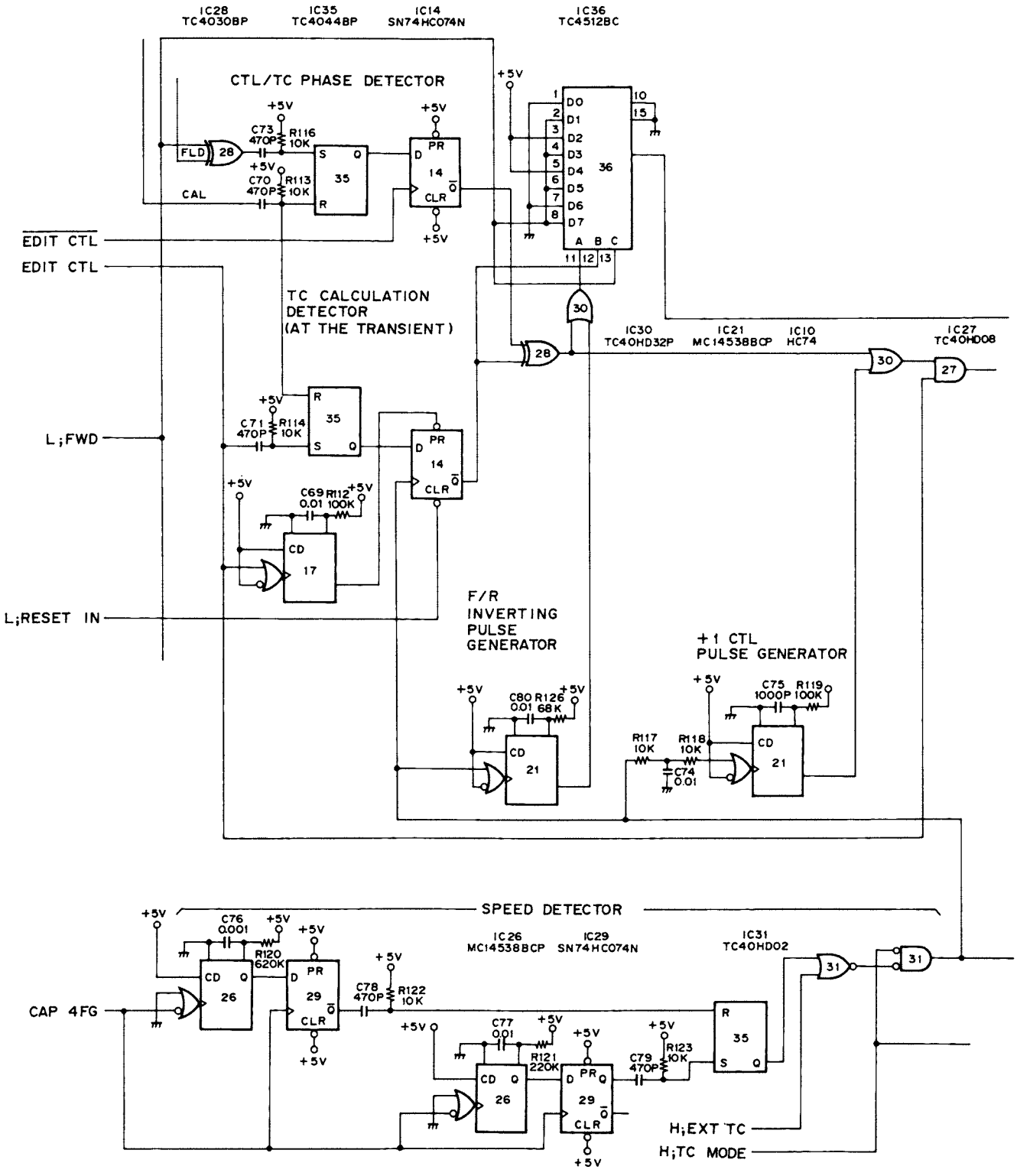


Fig.8-13. TC Reader Circuit

8-8-3. Data I/O

1. Data Bus Control

The 8-bit data bus is controlled using the 3-bit address bus by IC12 and 13.
Time code address bits 4, 5 and 6 are input to the decoder (IC12, IC13). Table 8-4 shows the statuses of the address and data buse. When, for instance, the time code address 4 is low, 5 is high and 6 is low and when the WR signal is simultaneously low, IC18 which is connected to the data bus latches the data. Information is thus sent to the time code generator IC2.

MODE	ADDRESS A4	A5	A6	DATA BUS STATUS
$\overline{RD}$	L	L	L	Data from the reader is latched.
	H	L	L	Status output from the reader is latched.
	L	H	H	Data from the RAM which is connected to generator is loaded.
$\overline{WR}$	L	L	L	Command sent to the reader is latched.
	L	H	L	(a) Command sent to the generator is latched.
	H	H	L	(b)
	L	L	H	(c)
	L	H	H	Data is written into the RAM connected to generator.

Table 8-4. Status of Address Bus and Dara Bus

2. Data Communication Between System Control and RAM

When the Table 8-4 address bus lines 4, 5 and 6 are low, high and high, respectively, the contents of the data communication corresponding to the address low-order 3 bits will be as shown in Table 8-5.
When the time code addresses 4, 5 and 6 are low, high and high, respectively, and the WR signal is low, low output of pin 50 of IC2 is supplied to pin 2 of IC30, which makes it possible to write the data into the RAM IC4. The addresses are controlled at this time by the switcher IC23.

3. Sending Commands to Time Code Generator and Reader

When the Table 8-4 address bus lines 4, 5 and 6 are low/low/low, low/high/low, high/high/low or low/low/high, respectively, commands are sent to the time code generator and reader.
The commands for sending to the time code generator are latched by IC18, 19 and 20.

4. Setting the Status Information Into System Control

When the Table 8-4 address bus lines 4, 5 and 6 are high, low and low, respectively, the status information is accepted in the system control circuit. When they are high, low and low, respectively, IC16 is controlled and the data is accepted. IC16 is used to transfer the time code reader error information and CF information to the data bus.

Address Bus Line No. 0	1	2	3	AD3	Data Bus Line 0 1 2 3	4 5 6 7
L	L	L	H	H	1 Frame	10 Frame
H	L	L	H	H	1 Sec	10 Sec
L	H	L	H	H	1 Min	10 Min
H	H	L	H	H	1 Hour	10 Hour
L	L	H	L	L	U-bit 1	U-bit 2
H	L	H	L	L	U-bit 3	U-bit 4
L	H	H	L	L	U-bit 5	U-bit 6
H	H	H	L	L	U-bit 7	U-bit 8

Table 8-5

8-8-4. Character Generator Circuit

The TC-42 board contains a circuit for generating the characters of time code and titles which are superimposed onto the video signals. This circuit is composed of the character generator IC, sync separator circuit and mode control circuit.
The sync signal corresponding to the VTR mode is selected by the switcher IC7. The horizontal sync signal is separated from the composite sync signal by IC6 and the vertical sync signal by Q3 and the low-pass filter, and they are supplied to the character generator IC5.
The character generator generates the background signals and character signals that correspond to the D0 through D8 character data which have been sent from the system control circuit, and it sends these signals to the video circuit.

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